Using Controlled Experiments in Layout

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Abstract: Since mathematically optimal layout algorithms seem unattainable, layout needs to become a more experimental science. This paper advocates the use of controlled experiments in layout. The physical design workshop bench mark layout environment, open problems solvable by experiment, and the relation of layout experiments to scientific methodology are discussed. The paper concludes by showing that layout synthesis of primitive cells by computer program is impossible since it is no easier than the general artificial intelligence problem.

Categories: 3.5 (layout), 3.1 (placement), 3.2 (routing)

1. Introduction

In a perfect world, there would exist provably efficient integrated circuit (IC) layout algorithms. Unfortunately, in reality most layout algorithms are NP complete [5]. There is even a lack of consensus concerning what makes one circuit layout superior to another. Final circuit area is probably most important, but among numerous conflicting criteria, electrical characteristics, congestion, via number, timing, and power distribution must be considered. Progress in such unstructured problem domains can often be facilitated by means of scientific experiments. The purpose of this paper is to advocate systematic experimentation in placement and routing.

To understand the need for layout experimentation, one must analyze the traditional engineering development methodology. A development project implements a system that ultimately becomes part of a larger manufacturing system. In the case of IC layout, the system includes computer programs, mask set manufacturing, and organizational procedures. Until the 1980s an electronic development project needed only apply the body of electronic circuit theory (physics of electromagnetism), but during the last decade IC digital circuit design has changed so that geometric (or combinatorial) component arrangement and electronic component connection have become the central design problems. This change was brought about by a large increase in the number of transistors that could be packed into a given area. Layout lacks the rules of thumb, background knowledge, and algorithm class intuitive characterizations that exist for electronic circuits. Knowledge gained from decades of experimental study of semiconductor devices. This paper argues that the academic study of layout ought to mean careful and controlled scientific measurement of layout algorithms and organizations. This experimentation should produce the body of theoretical knowledge required by industrial development projects. Imagine how little progress would have been made in transistor

development if only the mathematics of differential equations and algebra, but no electromagnetic physical theory, had been known. Sections 2.2 and 2.3 discuss the relation of layout experiments to scientific methodology. Section 3 discusses experimental opportunities. Section 4 describes an example experiment which suggests that adding a third metal layer beyond the normal two layers to a master slice substrate does not significantly reduce final circuit area. This result is surprising since most substrates are designed with this extra metal layer.

A necessary prerequisite for experimentation is the existence of simplified experimental systems and circuit designs that can be used in controlled experiments. In channel routing interesting problems have been available since 1976 [3]. The problem specification for channel routing connections is simple enough so that a problem description needs just a one or two page net list [3] [24]. The availability of universally available and default test cases has led to the development of a number of good channel routers all using different approaches (see for example [1] [22] [23] [32]). Even though channel routing can still benefit from controlled experiments that explain what aspects of the different algorithms account for their advantages, channel routing will not be discussed further since considered in isolation, it is mostly a solved problem.

Creation of a simplified experimental system for general layout is more difficult since any complete layout system contains hundreds of factors that mayor may not be relevant for layout algorithm development. Any simplified experimental system must at least define substrate organization, the primitive cell library, and routing geometric constraints. A large data file is required to define each of these layout system aspects. Section 2 discusses a layout test circuit environment along with a few individual test designs that have served as a simplified experimental system for the master slice layout problem. The environment and circuits were compiled for the physical design workshops [4] [21] [19]. Unfortunately, instead of using test circuits as an opportunity to learn more about layout, they have been used predominantly to provide test cases for competition between the placement and global routing parts of layout programs. The test circuits are even called ’benchmarks’ implying their universal nature rather than ’test circuits’ emphasizing the importance of treating each circuit, itself, as an object of study. A consensus rating order of layout programs has arisen based on the effectiveness of the systems on only a few circuits of small to medium size. There is also a tendency to believe that the general approach used for each part of the current best system (placer, global router, etc.) is also the best general algorithm. Section 2.1 discusses problems with layout test system applications.

Section 5 discusses a limitation of the experimental method. Even though controlled experiments are important, there are situations for which experiments do not contribute to the growth of knowledge since a problem can be shown by argument alone to be infeasible. Section 5 shows that layout synthesis of macro cell transistor layouts (mask pattern generation) is impossible since it is no easier than the general artificial intelligence problem. Since solution of the general artificial intelligence problem (replacement of common sense knowledge by a program) is unlikely in the foreseeable future, there is no need for experimentation and for that matter development. This is important since macro cell layout synthesis is commonly advocated as the next area of

layout progress. The physical design workshop name has even been changed to 'layout synthesis.'

2. The Simplified Layout Experimental System

The simplified layout environment has facilitated growth in placement and global routing because it retains the essential aspects of layout problems while omitting the numerous details required by a commercial circuit design environment. The YAL language [31] has proven effective in coding net lists, cell libraries, and placements because it is tailored to the algorithm development environment (see [17] for a discussion of problems with generalized net list coding schemes), and because the level of abstraction has proven to be suitable. The omission of technology dependent factors such as cell electrical function, pin pair wire segment decomposition, via representation, and mask geometric details has not caused difficulties. The macro cell library includes enough different cell types to allow nearly any circuit to be coded, yet avoids the complexity of the hundreds of different macro cells that would be required by a commercial system. The inclusion of cell blockages and requirements for correct feed through handling has allowed progress in global routing problems that were rarely dealt with before the advent of the layout test circuits [12].

The mere existence of layout tests is valuable since within the IC system design area far too many results have previously used only anecdotal evidence (see for example [10], pp. 26-28, 30). It is true that layout algorithms were compared before the test circuits were available (see [6] [7] [8] for example), but the pre layout test environment work compared published algorithms as implemented for one particular layout system. When results for a technique did not match the algorithm originator's claims, the discrepancy could usually not be explained. But even this primitive comparison methodology proved valuable since it led to the commercial systems ([8] [15] [25]) that still have laid out the vast majority of ASICs. At least at LSI Logic during development in the 1980s of the original algorithms, availability of the current layout test circuit comparisons would have been valuable since placement and routing were different computer programs for which different corporate entities were responsible [15]. This made total layout system comparisons somewhat problematic since both the placement program and global router needed to work in conjunction with a separate program's effectively black box algorithm.

2.1 Current Layout Test Case Usage and Problems

Test circuits are primarily used as test cases during layout program development, for generating experimental results when new algorithms are described (see recent layout papers in DAC or ICCAD proceedings), and to hold competitions to choose the best (or few best) layout systems. These applications are interesting but they do not provide much help in guiding a semiconductor company in developing a layout system tailored to its commercial product lines. This product specific customization or parameter setting is currently required by even the most advanced academic algorithms (see, for example, [29], p. 44). Also, commercial systems always have product type specific requirements. Knowing that one program produces less area in the abstracted layout test environment is not of much use when developing a commercial system.

Even within the layout test environment, comparison problems have arisen. Some systems were routed with the UTMC router [25] in the 1987 and 1988 workshops while others used their own router. Even for systems that used the UTMC router, there were comparison problems. The UTMC router inserts one grid wide feed through cells where needed. Some of the placements required this feature, but some were made worse by it. Some placements achieved small area but required more feed throughs than the UTMC router was able to add. Those placements would probably, but not definitely, require more area after feed through addition. Various placements used a substrate size dictated by I/O pad geometry. These placements required larger area than was required by those which ignored I/O pads. The area determined from the circumference needed for I/O pads was much larger than the area required by internal cells. See [5, p. 127] and [33, figure 5] for other comparison problems.

Comparisons according to final area also have methodological problems. It is possible for a system using an inferior algorithm but a better implementation to produce less area than what seems to be a better algorithm for which the implementation or choice of approximations is problematic. If an algorithm works poorly, it is currently not possible to isolate the reason. It could be an implementation mistake, a hidden background factor that caused the algorithm to be specialized to the original layout system, or an algorithm problem. Without controlled experimentation it is it not possible to determine the reason for the better or worse results. Finally, by competitively comparing area, develop of promising new algorithms may be halted early because early versions do not initially produce competitively small area. It is generally considered a mistake in research and development to put all effort into developing one approach to the exclusion of alternative approaches.

2.2 Proposed Layout Test Case Usage

This paper proposes that layout test circuits become the subjects of scientific experiments for which all aspects of the layout program are controlled except the one under study. Results are then reported using the normal scientific method. By presenting results in this manner, it allows new algorithms to be developed since the particular aspect for which they are superior can be presented. It also allows commercial layout system implementers to evaluate the value of algorithms independent of implementation quality. It may even allow general algorithmic questions to be answered which have importance beyond IC layout.

2.3 Relation to Scientific Methodology

It is possible to perform experiments in the layout test system that previous work in the methodology of science has identified as having importance for scientific growth. he most widely known condition first identified by Professor Kuhn requires the ability to solve puzzles [14]. There must be a way to decide within one approach (sometimes called a research program) if one technique is superior to another. For example, it should be possible to decide by scientific experiment within the simulated annealing research program if one annealing temperature schedule is superior to another. This requires the ability to control every possible variable and is possible in the simplified layout experimental system. Of course, in an area dealing with human design, a possible experimental result might be that one method is better for one design or substrate type

while another is better for another. The test circuits may provide the capability to systematically characterize such differences. This last sort of puzzle solving is known as problem shifting or problem splitting [11]. Another condition first identified by Professor Popper is the ability to falsify hypotheses (see [20] [11]). As a trivial example, without a controlled and widely available layout environment, it is impossible to falsify random placement. Imagine a claim of discovery that random placement with no evaluation function is superior to all other techniques. Without a controlled experimental system, the advocate of random placement could reasonably claim any falsification based on another implementation of random placement simply uncovered flaws in the implementation.

3. Experimental Opportunities

I believe study of the following experimental questions should provide the sort of theoretical knowledge required by industrial development of layout systems.

a. *Controlled algorithm comparison.*

Too much effort has been put into trying to produce improved layout systems without putting a corresponding amount of effort into attempting to understand what makes the system "good". The algorithm is usually named after the search strategy it uses, but it has not yet been shown that search strategy is a significant determinant of layout quality. Even the acknowledged best openly described layout systems still are effectively black boxes. For example, the success of Timberwolf [29] could as easily be related to the combination of placement and global routing into one process, as to the simulated annealing search strategy. It is not clear what aspect of quadrisection makes it work [30].

I believe many people would claim simulated annealing is the search strategy of choice, but this has never been proven. There is considerable negative evidence against its utility from formal studies. See [27] for a discussion of the weak mathematical power of simulated annealing. Also, in all the work that sought good searching heuristics, mostly for solving the traveling salesman problem, simulated annealing was not even considered (see for example [13]). Finally, many physical design workers still believe in continuous systems theory type approaches such as simulated annealing while those approaches are obsolete in nearly every other area of computer science. A controlled experiment that keeps all aspects of a layout system constant except for search strategy would be interesting. Of course, considerable ingenuity may be required to eliminate problems caused by algorithm aspects whose implementation is related to properties of simulated annealing. Hopefully, the experiments will be described in sufficient detail so that an industrial implementer can gain insight that allows the algorithm discoveries to be applied to a particular industrial problem. The industrial problem may be totally new due to an integrated circuit break through. This experimentation may have much wider applicability to heuristic search questions in general.

b. *Substrate organization comparison.*

It is possible to evaluate new or competing substrate organizations by holding the layout program and test circuit as constant as possible, and then varying the substrate organization upon which the circuit is laid out. Finally, the resulting layouts can be compared. The comparison may involve considerable ingenuity and intuition, but if the details are published, people will be able to decide for themselves. I believe too many product line substrate organization decisions in semiconductor companies are made according to how the advertising copy will read.

c. *Global and channel router interaction.*

The traditional layout approach separates the process into three steps: placement, global routing, and channel routing. It is possible to achieve channel routing densities near the theoretical minimum, but this minimum may interfere with global connections such as vertical wiring channel feed throughs. It would be interesting to determine the trade off between optimum channel routing and less dense channel routing that leaves room for global wiring. The idea would be to avoid using the channel router for global wiring but instead leave unoccupied wiring regions and use a separate and possibly iterative wiring approach. This approach is in contrast to the one that takes global router results and chooses the global entry and exit points for the in channel section of the global wire.

d. *Testing and improvement of the layout test environment.*

It is probable that once the simplified layout test system is used for controlled experiments, changes will be necessary in the environment and circuits. This process will be more efficient if controlled experiments are used to assist in deciding the changes that need to be made.

e. *Evaluation of heuristics and approximations in a controlled environment.*

There is considerable disagreement on which approximations can safely be made during placement or global routing and which can not. For example, it is still open whether it is sufficient to treat all nets as if they contained only two pins with possibly with correction factors applied for non two pin nets. Many developers believe using the net half perimeter is better. A few even believe only exact Steiner tree net measurements are acceptable. Experiments that keep everything constant but change the low level wire length calculations in the placement evaluation function would be interesting.

f. *Experiments to systematically classify circuits types.*

This area could be of particular value to commercial developers for products aimed at particular circuit types. It would be interesting to see results from experime;ts that measure in a controlled manner layout parameters for different circuit types. If it is possible to improve layout results given a known circuit class, this would have large economic value. On the other hand, I believe the current generation of layout programs has become too specialized to the physical design workshop primary1 3000 gate peripheral controller and the 8000 gate primary2 microprocessor circuits. Results from

different test circuits would be interesting.

4. Example Third Metal Layer Substrate Evaluation Experiment

In order to illustrate the experimental approach, an experiment measuring the possible utility of including a third layer of metal as part of a substrate organization. The experiment holds all factors fixed and then rewires a placement (at the global routing level) using three metal layers. It is interesting because the improvement from a third layer metal is seemingly not large. This experiment can, of course, be criticized since remapping a placement optimized for two layer metal may not be valid. The purpose of this example is to encourage more accurate experimentation.

A number of experimental master slice ASIC circuits use a third metal layer (metaI3). The most obvious use dedicates metal3 to long vertical cell row feed through wires (actually feed over) that connect pins on rows separated by an intervening cell rows. The connection pattern illustrated in figure 3 would use the third metal layer but the patterns shown in figures 1 and 2 would not. The advantage of dedicating metal3 to long vertical connections is that such wire cause no congestion in the regions they cross. The alternative of dedicating metal3 to horizontal wires suffers from the problem that the vias connecting metal1 and metal3 horizontal wires in, for example, channel jogs block scarce vertical metal2 feed through grids. There may be some better mixed direction metal3 use not considered here.

Known good circuit placements can be used to measure the possible benefit from dedicating metal3 to vertical wires. The results discussed here use placements made for two layer metal by the Timberwolf system [29] to see the amount of track and feed through reduction possible with simple rewiring. The Timberwolf 17 row primary1 and 23 row primary2 placements from the 1988 workshop are used. The next step would possibly be to repeat this experiment using placements from a placer modified to maximize vertical wiring. But since maximizing vertical wiring causes an increase in real wire length, the rewiring scheme discussed here may actually show the limit of potential size reduction from the addition of a third metal layer.

The following data measures YAL coded Timberwolf placements and uses a placement level routing estimate approach described in [16]. The routing estimate decomposes each net into pin pairs using the minimum spanning tree and then assumes the connection can be made with at most one via. Steiner MST decomposition does not materially change the results [16]. This measurement scheme gives an optimistic estimate of the gain from a third metal layer since if extra vias are needed, the long metal3 wires will cause additional congestion.

Tables 1 and 2 compare the rewired vertical feed through numbers for the primary1 and primary2 circuits to the original two metal layer wire requirement where the spanning tree pin pair decomposition used exact physical wire length rather than weighing to maximize vertical wires. For exact physical wire length, a wire connecting rows separated by two intervening wiring channels and one cell row (see figure 3) along one vertical grid is as distant as a pin connecting to another pin 60 grids (20 gates) distant along the same row (see figure 1). For the three metal layer vertical wire maximizing measurement, the spanning tree distance metric assumes the same vertical connection is

equivalent to a pin only six grids (two gates) distant. Further decrease in vertical wire cost leads to no increase in horizontal wiring and no channel height decrease at least for the two physical design workshops primary test circuits. Column two contains the required vertical feed through wire number for each row for the two layer metal case. Column three gives the percentage of available feed through used. Available means non blocked metal2 grids and assumes no vertical feed throughs would be lost to congestion problems.

To understand the meaning of column three, consider the most congested primary2 row 17. The required 1039 feed through wires is 23.7 percent more than available because the 23 row placement row length is 1005 grids of which 165 are blocked by vertical intracell wiring or unconnected pins (only 14). The percentage used is 1039/840 or 123.7. A value of more than 100 percent means a possible feed through shortage that requires either additional feed through cells which would lengthen every row or a better global routing approach. Column four gives the number of long vertical wires possibly movable to metal3. Column five gives the percentage of metal3 feed throughs that would be used above each row if every possible wire were moved to metal3.

Since the primary circuit has available feed throughs, adding a third metal layer does not lead to significant area reduction. Nearly two thirds of the available metal3 feed through grids are unused over most internal rows. Global routing that makes maximum use of metal3 would, at a minimum, reduce the number of required track from 226 to 209 or 7.5 percent. The trade off is a 10.4 percent increase in total wire length. This assumes the layout test system uses the same pitch for all metal layers. A better global router could reduce the required maximum channel density by moving wires into horizontal channel sections with unused grids below the maximum channel requirement thereby reducing channel density peaks, but then the same router could probably also reduce peaks in the two layer metal case [12].

Table 2 shows the saving for the primary2 circuit. The advantage of a third metal layer for the primary2 circuit is potentially larger since there is a shortage of metal2 vertical feed through tracks (see table 2 column 3). It is possible that a global router that changes connecting pin pairs to reduce vertical feed through requirements by using wiring channel sections below maximum channel density could possibly route the rows with a shortage of feed through. If the improvement is not possible, a global routing that maximizes use of metal3 would, at a minimum, reduce horizontal routing channel tracks from 544 to 486 or 10.7 percent. The trade off is a 15.1 percent increase in total wire length. Column five shows that more than half of the available metal3 tracks are used over the central rows and also that around half of the metal2 feed through tracks are unused. If all the master slice row lengths really need to be increased by the 199 grids required by row 17 in the two metal layer case, addition of a third metal layer can reduce total area by 25 percent (1005/1204*486/544). Of course, the actual decision to add a third metal layer will be determined by manufacturing and electrical considerations. Finally, since this experimental methodology applied here does not apply to four metal layers, it would be interesting to determine the advantage of adding two extra metal layers.

5. Impossibility of Cell Primitive Synthesis

Cell generation (sometimes called cell layout synthesis) differs from other layout problems that assign macro cells and wires to substrate locations in the sense that it is not an optimization problem solvable in principle if computers were fast enough to overcome the limitations of NP completeness. Rather, it is an unstructured intuitive problem that is no easier than the general human intelligence problem. Examples of this general problem are natural language understanding, scientific discovery, and legal decision making, but not chess. Since it is not possible to abstract out a formal problem and be sure solving the formal problem also solves the intuitive cell synthesis problem, successful cell generation computer programs are no more likely than successful natural language understanding programs. Fortunately, human primitive cell design is not particularly difficult since cells are small and at most a few hundred are needed for any given product line.

There are a number of ways to view the general intelligence problem. One view characterizes it as an intuitive problem for which all human scientific and cultural background knowledge can be brought to bear. Another characterization is as a problem that requires balancing of conflicting requirements such that any algorithm for balancing can be beaten by intuitive knowledge. Another viewpoint defines the problem as one of meaning rather than syntactic understanding ([28], p. 31-32). According to this view, is necessary to understand in an intuitive, gestalt, unconscious, subconscious, and even formalist sense all at once.

The cell synthesis problem is equivalent to the general intelligence problem since it requires the balancing of a number of conflicting requirements, is amenable to scientific progress since completely new circuits designs can be discovered using the background knowledge embedded in solid state physics, requires subtle intuitive judgment, and finally is a problem whose solution is improved by human trial and error experience. The following conflicting requirements must be balanced and 'synthesized' (used in the informal sense here) into a circuit represented finally as a mask set. These conflicting criteria, which are embedded in the conceptual matrix of circuit electrical parameters (resistance, capacitance, stability, etc.) and manufacturing process technology, must be combined and balanced. Cells need porosity for feed through wires yet can not be too porous or area and speed will be inefficient. Cell interfaces must be well behaved since future electrical environment is only predictable in an intuitive sense, yet too many buffers will again result in inefficient cells. The advantages of the small area and delays of pass transistors must be balanced against unpredictable delays and a tendency to become bidirectional (an expert would run spice experiments to determine if pass transistors are acceptable in a given place). Cell power distribution simplicity (resulting in small area) must be balanced against substrate area, electrical field, and magnetic field characteristics of an entire chip's power bus distribution system. Geometric design rules that require large area must be balanced against smaller but potentially unreliable intuitive circuit feature patterns in an environment of changing process manufacturing methods and parameters. Second, the recent rapid growth in ASIC technology switching delays minimization and area reduction (outside of process feature size shrinkage) has been made possible by scientific discoveries [2] which are not algorithmic in nature. Finally, experienced cell designers produce both smaller and faster cells than experts with

similar background but no experience.

6. References

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Tables and Figures

	Real Wire Distance		Two Rows Equal Two Gates	
Cell Row	Total Crossing Wires	% of Metal2 if no Metal3	Possible Metal3 Wires	%s of Metal3
1	188	57.7	33	6.9
2	243	73.3	48	10.1
3	223	70.8	68	14.1
4	286	85.5	120	25.1
5	279	84.3	144	29.9
6	283	83.4	177	36.9
7	291	88.2	195	40.5
8	324	94.1	208	43.2
9	334	95.7	192	40.0
10	307	89.7	176	36.6
11	324	94.2	153	31.8
12	284	86.3	137	28.5
13	263	82.1	119	24.8
14	252	77.2	102	21.3
15	246	74.7	78	16.2
16	227	68.8	50	10.4
17	220	67.9	24	5.0

TABLE 1. Primary1 Metal3 Vertical Feed Through Wires

	Real Wire Distance		Two Rows Equal Two Gates	
Cell Row	Total Crossing Wires	% of Metal2 if no Metal3	Possible Metal3 Wires	%s of Metal3
1	478	63.9	128	12.8
2	633	79.4	221	22.0
3	715	90.2	297	29.5
4	700	88.0	346	34.4
5	802	97.4	408	40.6
6	833	100.7	430	42.7
7	938	110.5	448	44.5
8	896	107.2	500	49.8
9	923	91.7	520	51.7
10	890	107.4	535	53.2
11	858	105.0	583	58.0
12	839	104.6	560	55.7
13	953	117.0	574	57.1
14	901	108.6	558	55.5
15	944	113.7	537	53.4
16	983	116.5	553	55.0
17	1039	123.7	566	56.3
18	1008	117.2	576	57.3
19	929	109.5	535	53.2
20	847	102.1	445	44.2
21	821	97.5	359	35.7
22	755	91.8	208	20.7
23	549	74.8	94	9.4

TABLE 2. Primary2 Metal3 Vertical Feed Through Wires

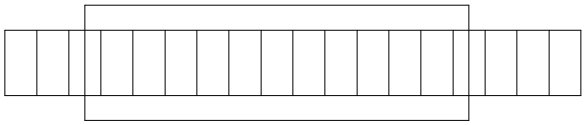

Figure 1. Along Channel Possible Connections

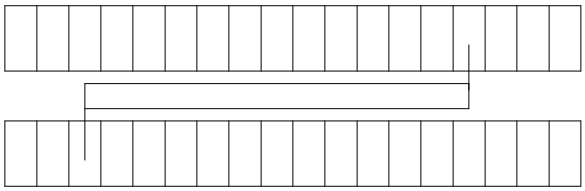

Figure 2. Cross Channel Connection

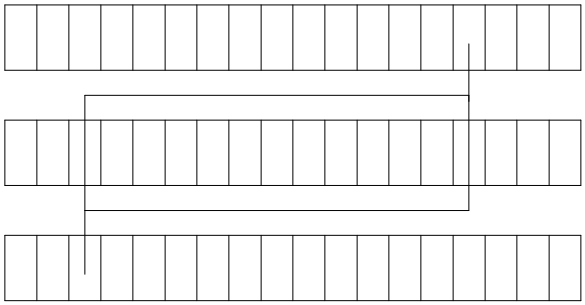

Figure 3. Cross Row One Via Possible Connections