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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/899,763	07/05/2001	Steven J. Meyer	~~2470.02US02~~ 3022.024US02	2544

24113 7590 07/27/2005

EXAMINER	
OSBORNE, LUKE R	

ART UNIT	PAPER NUMBER
2123	

PATTERSON, THUENTE, SKAAR & CHRISTENSEN, P.A.
4800 IDS CENTER
80 SOUTH 8TH STREET
MINNEAPOLIS, MN 55402-2100

DATE MAILED: 07/27/2005

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AUG 01 2005
PATTERSON, THUENTE, SKAAR
& CHRISTENSEN, P.A.

DOCKETED

Please find below and/or attached an Office communication concerning this application or proceeding.

Date of Office Action 7.27.05
Response due 10.27.05
Per 1 month extension 11.27.05
Per 2 month extension 12.27.05
Per 3rd and FINAL extension 1.27.06

PTO-90C (Rev. 10/03)

Docketing Review 8-4-05

Office Action Summary	Application No.	Applicant(s)	
	09/899,763	MEYER, STEVEN J.	
	Examiner	Art Unit	
	Luke Osborne	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/19/02, 9/2/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Status

1. Claims 1-44 are pending in the instant application.

Claims 1-44 stand rejected.

Information Disclosure Statement

2. The information disclosure statement (IDS) submissions on 4/19/02, 9/2/03 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 15-29 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

For a claimed invention to be statutory, the claimed invention must be within the technological art. Mere ideas in the abstract (i.e., abstract idea, law of nature, natural phenomena) that do not apply, involve, use, or advance the technological art fail to promote the "progress of science and the useful arts" (i.e., the physical sciences as opposed to social sciences, for example) and therefore are found to be non-statutory subject matter. For a method claim to pass muster, the recited process must somehow apply, involve, use, or advance the technological arts.

As to technological arts recited in the preamble, mere recitation in the preamble (i.e., intended or field of use) or mere implication of employing a machine or article of manufacture to perform some of the recited steps does not confer statutory subject matter to an otherwise abstract idea unless there is positive recitation in the claim as a whole to breathe life and meaning into the preamble. In Bowman (Ex parte Bowman, 61 USPQ2d 1665, 1671 (BD. Pat. App. & Inter. 2001) (Unpublished), the board affirmed the rejection under U.S.C. 101 as being directed to non-statutory subject matter. Although Bowman discloses transforming physical media into a chart and physically plotting a point on said chart, the Board held that the claimed invention is nothing more than an abstract idea, which is not tied to any technological art or environment.

In the present case, although claim 15 recites at the preamble a method of analog mixed signal simulation for simulating a circuit, having both digital and analog components, that is described by one or more hardware description languages (HLDs), the steps in the claim body of reading, elaborating the analog and digital components and initializing, can be implemented by the mind of a person or by the use of a pencil and paper. In other words, since the claimed invention, as a whole, is not within the technological arts as explained above, these claims only constitute an idea and does not apply, involve, use, or advance the technological arts, thus, it is deemed to be directed to non-statutory subject matter.

Examiner suggests the addition of –computerized—or –computer implemented— in front of method for claim 15.

Any claim not directly rejected on 35 U.S.C 101 stands rejected due to its dependency.

To expedite a complete examination of the instant application, the claims rejected under 35 U.S.C 101(nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-44 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,560,572 to Balaram et al hereafter "Balaram."

Regarding claim 1 Balaram teaches a system for simulating a circuit having both digital and analog components, wherein at least a portion of said circuit has been coded into a hardware description language (HDL) model. See Figures 2, 4, 7 and the corresponding portions of Balaram's specification for this disclosure. In particular, Balaram teaches a system for simulating a circuit having both digital and analog

components, wherein at least a portion of said circuit has been coded into a hardware description language (HDL) model, comprising:

– a digital simulator (event driven simulator) that utilizes a programming language interface (PLI), (parameter passing) wherein said digital simulator produces digital circuit information based on said HDL model [The parameter passing portion 11 receives parameters from the circuit simulator 3 and return parameters to the simulator 3, through the user-defined modeling feature 7.(Column 3, lines 38-40)];

– an analog simulator (circuit simulator) that utilizes said PLI, wherein said analog simulator produces analog circuit information based on said HDL model [The netlist 36 describing the circuit is created by a user. The netlist 36 is fed to XSPICE simulator 30. The XSPICE simulator 30 uses built-in devices 38 of XSPICE as well as devices externally described with code modeling to simulate the circuit. (Column 4, lines 61-67)]; and

– a mixed signal program that utilizes said PLI, that controls said digital and analog simulator, and that synchronizes a discrete digital time and a continuous analog time, wherein the use of said PLI by all three of said digital simulator, said analog simulator, and said mixed signal program comprises a mixed signal engine

[Referring to FIG. 4, the steps to how the simulators are linked are: A. The code model 34 is fed stimulus by the XSPICE simulator 30 B. This stimulus is fed via the code model 34 to the HDL simulator 32 C. The HDL simulator 32 calculates the appropriate response D. The response is returned to the code model 34 E. The code model 34 returns the response back to the XSPICE simulator 30 (Column 5, lines 22-32)]" as claimed.

Regarding claim 2, Balaram teaches the system of claim 1, "wherein said digital simulator includes an elaborator, wherein said elaborator converts a digital portion of a circuit net list description into an internal digital and instance structure database within said digital simulator [Figure 3, item 32, HDL Chip Design into the HDL Simulator], and wherein said analog simulator includes an elaborator, wherein said elaborator converts an analog portion of a circuit net list description into an internal database within said analog simulator [Figure 3, item 30 ,36]" as claimed.

Regarding claim 3, Balaram teaches the system of claim 2, "wherein said mixed signal program operates to read the digital simulator database and transfer the digital simulator database to said analog simulator, wherein said mixed signal program operates to read the analog simulator database and transfer the analog simulator database to said digital simulator, and wherein said mixed signal program utilizes the read data within the digital simulator database and the analog simulator database to perform a mixed signal interface processing function

> [Referring to FIG. 4, the steps to how the simulators are linked are: A. The code model 34 is fed stimulus by the XSPICE simulator 30 B. This stimulus is fed via the code model 34 to the HDL simulator 32 C. The HDL simulator 32 calculates the appropriate response D. The response is returned to the code model 34 E. The code model 34 returns the response back to the XSPICE simulator 30 (Column 5, lines 22-32)]" as claimed.

Regarding claim 4, Balaram teaches the system of claim 1, "wherein said digital simulator includes an event engine to schedule a discrete time digital event

> [Referring to FIG. 4, the steps to how the simulators are linked are: A. The code model 34 is fed stimulus by the XSPICE simulator 30 B. This stimulus is fed via the code model 34 to the HDL simulator 32 C. The HDL simulator 32 calculates the appropriate response D. The response is

returned to the code model 34 E. The code model 34 returns the response back to the XSPICE simulator 30 (Column 5, lines 22-32)]" as claimed.

Regarding claim 5, Balaram teaches the system of claim 1, "wherein said analog simulator includes an analog circuit equation solver

[Referring to FIG. 4, the steps to how the simulators are linked are: A. The code model 34 is fed stimulus by the XSPICE simulator 30 B. This stimulus is fed via the code model 34 to the HDL simulator 32 C. The HDL simulator 32 calculates the appropriate response D. The response is returned to the code model 34 E. The code model 34 returns the response back to the XSPICE simulator 30 (Column 5, lines 22-32)]" as claimed.

Regarding claim 6, Balaram teaches the system of claim 1, "further comprising a time synchronizer that enables said mixed signal engine to schedule a PLI call back, wherein said PLI call back stops a digital simulation by said digital simulator so that said continuous analog time can advance to said discrete digital time or can move to a synchronization point

[SPICE simulators, of which an XSPICE simulator 30, is a subset, can move forward and backward in time as they try and retry possible directions. In order to interface to an HDL simulator which only has a concept of moving forward in time, several calls are added to save an old successful state for later use in the event the simulation fails. (Column 6, lines 65- Column 7, line 3)]" as claimed.

Regarding claim 7, Balaram teaches the system of claim 1, "further comprising a time synchronizer that enables said mixed signal engine to return from a PLI call back, wherein upon returning from said PLI call back, said digital simulator is advanced enabling said discrete digital time to advance to said continuous analog time or can move to a synchronization point

[SPICE simulators, of which an XSPICE simulator 30, is a subset, can move forward and backward in time as they try and retry possible directions. In order to interface to an HDL simulator which only has a concept of moving forward in time, several calls are added to save an

> old successful state for later use in the event the simulation fails. (Column 6, lines 65- Column 7, line 3)]" as claimed.

Regarding claim 8, Balaram teaches the system of claim 1, "further comprising a digital value changer that enables said mixed signal engine to schedule a value change call back on a digital signal, wherein upon a change in said digital signal said value change call back enable said mixed signal engine to change said digital signal to an analog value

> [A solution is to turn the HDL simulator 32 states into their analog equivalent (D to A bridging). The digital device is then seen in the XSpice simulator 30 circuit as an analog device. Stimulus is fed to the code model 34 from the HDL simulator 32 as a digital signal. The code model 34 then translates this to an appropriate signal for input to the XSpice simulator 30. A corresponding analog to digital conversion occurs when stimuli are sent from the XSpice simulator 30 through the code model 34 to the HDL simulator 32. The D to A and A to D conversions are implemented in the code model 34 in a manner known to those skilled in the art. (Column 5, lines 52-62)]" as claimed.

Regarding claim 9, Balaram teaches the system of claim 1, "further comprising an analog to digital converter that enables said mixed signal engine to determine a digital value from an analog wave form pattern

> [A solution is to turn the HDL simulator 32 states into their analog equivalent (D to A bridging). The digital device is then seen in the XSpice simulator 30 circuit as an analog device. Stimulus is fed to the code model 34 from the HDL simulator 32 as a digital signal. The code model 34 then translates this to an appropriate signal for input to the XSpice simulator 30. A corresponding analog to digital conversion occurs when stimuli are sent from the XSpice simulator 30 through the code model 34 to the HDL simulator 32. The D to A and A to D conversions are implemented in the code model 34 in a manner known to those skilled in the art. (Column 5, lines 52-62)]" as claimed.

Regarding claim 10, Balaram teaches the system of claim 1, "further comprising a digital to analog converter that enables said mixed signal engine to determine an analog value from a digital value

> [A solution is to turn the HDL simulator 32 states into their analog equivalent (D to A bridging). The digital device is then seen in the XSpice simulator 30 circuit as an analog device. Stimulus is fed to the code model 34 from the HDL simulator 32 as a digital signal. The code model 34 then translates this to an appropriate signal for input to the XSpice simulator 30. A corresponding analog to digital conversion occurs when stimuli are sent from the XSpice simulator 30 through the code model 34 to the HDL simulator 32. The D to A and A to D conversions are implemented in the code model 34 in a manner known to those skilled in the art. (Column 5, lines 52-62)]" as claimed.

Regarding claim 11, Balaram teaches the system of claim 1, "wherein said digital simulator maintains a digital database and said analog simulator maintains an analog database, and wherein said mixed signal engine is able read a value from and write a value to said digital database and said analog database

> [Referring to FIG. 4, the steps to how the simulators are linked are: A. The code model 34 is fed stimulus by the XSPICE simulator 30 B. This stimulus is fed via the code model 34 to the HDL simulator 32 C. The HDL simulator 32 calculates the appropriate response D. The response is returned to the code model 34 E. The code model 34 returns the response back to the XSPICE simulator 30 (Column 5, lines 22-32)]" as claimed.

Regarding claim 12, Balaram teaches the system of claim 11, "wherein the writing of said mixed signal engine to said digital database or said analog database provides for simulation control

> [Referring to FIG. 4, the steps to how the simulators are linked are: A. The code model 34 is fed stimulus by the XSPICE simulator 30 B. This stimulus is fed via the code model 34 to the HDL simulator 32 C. The HDL simulator 32 calculates the appropriate response D. The response is returned to the code model 34 E. The code model 34 returns the response back to the XSPICE simulator 30 (Column 5, lines 22-32)]" as claimed.

Regarding claim 13, Balaram teaches the system of claim 12, "wherein said simulation control comprises a digital control script [A device is specified to the simulator 32 as a design program. The design program cannot run in isolation. It must be fed stimulus and list responses to be checked. Ordinarily, a test harness, not shown,

is written to test the device by providing the stimulus and expected responses. (Column 5, lines 1-6)]" as claimed.

Regarding claim 14, Balaram teaches the system of claim 12, "wherein said simulation control comprises an analog control script

> [In the example implementation, the code model 34 in XSPICE provides a test harness for the HDL simulator 32. The code model 34 talks to the HDL simulator 32 and provides the stimulus from the simulator 30 to the simulator 32 and returns the responses from the simulator 32 to the simulator 30. To the HDL simulator 32 this functions as a test harness. (Column 5, lines 15-21)]" as claimed.

Claims 15-29 recite the method limitations of system claims 1-14, thus are rejected for the same reasons as claims 1-14.

Claims 30-44 recite the system means for the system claims 1-14, thus are rejected for the same reasons as claims 1-14.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO form 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luke Osborne whose telephone number is (571) 272-4027. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LRO

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

FORM PTO-1449 MODIFIED

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

Docket No.: 3020.02US02	Application No.: 09/899,768
APPLICANT: Meyer	
FILING DATE: July 5, 2001	
GROUP ART UNIT: 2123	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4,792,913	Dec. 1988	Buckland et al.			
	4,985,860	Jan. 1991	Vlach			
	5,105,373	Apr. 1992	Rumsey et al.			
	5,297,066	Mar. 1994	Mayes			
	5,394,346	Feb. 1995	Milsom			
	5,471,409	Nov. 1995	Tani			
	5,481,484	Jan. 1996	Ogawa et al.			
	5,822,567	Oct. 1998	Takeuchi			
	5,991,522	Nov. 1999	Shoen			
	6,110,217	Aug. 2000	Kazmierski et al.			

EXAMINER SIGNATURE

DATE CONSIDERED 7/18/03

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	09/899,763
Filing Date	July 5, 2001
First Named Inventor	Meyer
Art Unit	2123
Examiner Name	Not Assigned
Attorney Docket Number	3020.02US02

Sheet 1 of 1

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
		Electronic Circuit Simulation in a Mixed-Language Environment, Litovski et al., Microelectronics Journal, Mackintosh Publications Ltd., Vol. 29, No. 8, August 1, 1998; pgs. 553-558.	
		Hardware Description Languages for ALECSIS Simulator, Damnjanovic et al., Microelectronics 1995 Proceedings, New York, IEEE, September 1995, pgs. 525-528.	
		Verilog-AMS Language Reference Manual, Open Verilog International, December 1999, Los Gatos, California, Chapter 9.	
		On the Design of Mixed-Mode Simulators for Modern VLSI Circuits, Abdallah et al., Circuits and Systems Proceedings 1995, New York, IEEE, August 1995, pgs. 1168-1171.	
		A System-Level Simulation Environment for System-on-Chip Design, Schneider et al., 13th Annual IEEE International ASIC/SOC Conference, September 2000, Washington, D.C., pgs. 58-62.	

EXAMINER SIGNATURE		DATE CONSIDERED	7/18/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 120 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Notice of References Cited	Application/Control No. 09/899,763	Applicant(s)/Patent Under Reexamination MEYER, STEVEN J.	
	Examiner Luke Osborne	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,535,223 A	07-1996	Horstmann et al.	714/744
	B	US-6,339,836 B1	01-2002	Eisenhofer et al.	716/5
	C	US-6,560,572 B1	05-2003	Balaram et al.	703/22
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Steve Meyer "Verilog Plus C Language Modeling with PLI 2.0: The Next Generation Simulation Language" Verilog HDL Conference and VHDL International Users Forum, 1998. IVC/VIUF. Proceedings.,16-19 March 1998 Page(s):98 - 105
	V	Force, C.; Austin, T., "Testing the design: the evolution of test simulation" Test Conference,18-23 Oct. 1998 Page(s):612 - 621
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.