The Master Slice Layout Bench Mark Experimental System

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Sincerely,

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Abstract: Since mathematically optimal layout algorithms seem unattainable, layout needs to become a more experimental science. This paper shows how the master slice bench mark circuits prepared for previous physical design workshops can be used as an experimental system for testing layout algorithms, systems, and substrate organizations. In this paper are discussed, the bench mark layout style, characterization of primary bench mark circuits, and the relation of layout experiments to scientific methodology. An example experiment using the bench mark system to evaluate area reduction from one possible use for a third metal layer is presented.

Categories:

Physical Design: Layout, Placement, Routing
Systems: CAD Development Methodology

1. Introduction

In a perfect world, there would exist provably efficient layout algorithms. Unfortunately, in reality most layout algorithms are NP complete [2]. There is even a lack of consensus concerning what makes one circuit layout superior to another. Circuit area is probably most important, but electrical characteristics, congestion, via number, and timing must be considered. Progress in such unstructured problem domains can often be facilitated by means of scientific experiments. A set of bench mark circuits available from the Microelectronics Research Center of North Carolina can act as a simplified experimental system for master slice layout program and circuit substrate development. The circuits were originally developed for the 1987 and 1988 Physical Design Workshops [1] [14]. A master slice based IC is either a standard cell, gate array, or sea of gates circuit organized as fixed width cell rows separated by horizontal wiring channels with at least two perpendicular metal wiring layers. Vertical feed through are used for row crossing connections. The terms row based or cell based are sometimes used as synonyms for master slice. There are a number of non master slice circuit design approaches such as general cells or full custom silicon structures that are not discussed here since comparisons between different design styles for which there are no common primitives is beyond the scope of scientific experimentation. Master slice circuits make up the vast majority of non commodity ICs.

The bench mark experimental system consists of a macro cell library, substrate specifications, and bench mark circuits coded using the YAL language [19]. The master slice bench mark layout system is a simplified experimental system in three senses: macro cell electrical function is not specified, wire segments and vias are not represented, and mask geometry details are not dealt with. This level of circuit representation is commonly used by placement and global routing programs. For an overview of the complete master slice design and layout process see [12] or [18]. The idea to compare various layout approaches is not new (see [3] [4] [5] for example), but previous work

compared published algorithms as implemented for one particular layout system. When results for a technique did not match the algorithm originator's claims, the discrepancy could not be explained. The bench mark system allows such comparisons to be made in a controlled environment.

The purpose of this paper is to advocate use of the bench mark experimental system in systematic experiments rather than simply as test cases for layout program development. This paper begins by describing the bench mark layout style. This material shows that the bench mark experimental system closely models layout system aspects of common commercial ASIC circuits. Next, the relation of bench mark experiments to scientific methodology is discussed. An example scientific experiment is presented that measures the potential benefit of one possible use of a third metal layer. Finally, open problems, limitations of the system, and possible improvements are discussed.

2. Bench Mark Layout

Bench mark circuits are composed of rows of macro cell primitives layed out in a rectangular region on a master slice style chip substrate [12]. The rows are separated by horizontal wiring channels and I/O pads surround all four sides of the master slice area. The three most common types of digital application specific integrated circuits are gate arrays, standard cells, and sea of gates. The bench mark experimental system can be applied to all three circuit types and can be used to compare differences since during the back end layout phase, the three approaches differ only in variability of wire channel height and of feed through width.

The most general standard cell style can be converted into a gate array or sea of gates by widening explicitly added feed through cells from one wire grid to one gate (three grids), by rounding macro cell widths up to the next integral gate number, and by fixing wiring channel height for gate arrays or by specifying half cell row height for sea of gates [6]. Since this is a simplified experimental system, even for gate arrays, wiring channel height need not be fixed in advance. Even though in theory a layout system can determine the number and length of rows for the standard cell approach, in practice those values are usually determined from packaging requirements or by trial and error. Standards cells in principle allow more variability such as variable length rows, variable height macro cells, and jagged wiring channels, but this variability is not used. In effect, the various master slice design styles have undergone convergent evolution.

All I/O pad cells are preplaced into fixed substrate slots that are about the same width as two flip flops (30 wire grids). The use of preplaced I/O pads is realistic since the combination of system board level pin out requirements and electrical requirements rarely leave much pad location assignment leeway. The bench mark system uses a first metal layer (metal1) for horizontal wires and a second metal layer (meta12) for vertical feed through wires. Metal vias connect the two layers. First level metal inside macro cells is reserved for horizontal intracell connections. Horizontal connections between macro cells must use routing channels. Second level metal vertical wires must either feed through unoccupied locations in cell rows or run around row ends. Wires can feed through cell rows in one of three ways. If a wire needs to connect to a terminal, it can enter the cell on the top or bottom, connect to the terminal, and leave on the other side.

Second, a wire can be routed through a cell row using an explicitly added one grid wide (3 for gate arrays) feed through cell inserted between cells. Finally, a wire can feed through an unoccupied wire grid within a cell. Grids are occupied if they contain a macro terminal or are blocked by a vertical intracell wire required for transistor connections. Generally, only macro cells that implement sequential logic contain blockages. The availability and location of feed through grids is coded in the macro cell library. Since in the current bench mark library, every macro cell terminal is on metal2, it is impossible to feed vertical wires through grids that contain unconnected terminals. Terminals should possibly be moved to metal1 since an increase in available feed through of up to about five percent is sometimes achievable.

2.1 The Macro Cell Library

The bench marks library includes 15 macro cells. All macro cell have uniform height and are an integral number of wire grids wide. Two pins in one macro cell never lie along the same vertical grid, and the library is specified such that it is only necessary to connect to the edge of a horizontal wiring channel at a vertical grid to connect to a pin. Cell rows can be treated as horizontal lines without loss of generality.

Internal macro cells are named according to their type and I/O terminal counts. Combinatorial gates (simple nands and nors) start with the letter G while sequential flip flops and latches start with the letter F. The letter is followed by two numbers. The first is the number of cell inputs, and the second is the number of cell outputs. For example, an inverter is named G11, any two input combinatorial gate G21, and a standard D flip flop with set and clear or a scan D flip flop with no presets are called F42. Electrical function is removed from macro cells by using one macro for all circuits with a given number of inputs and outputs. I/O pad macro cells start with a letter indicating their direction (I for input, O for output, or B for bidirectional) followed by an arbitrary number.

The library contains only small macro cells. The largest (widest) cells are G81 using 16 grids (18 for gate arrays) and F42 using 20 grids (21 for gate arrays). If a three of eight decoder or similar complex macro cell were in the library, approximately 150 grids (50 gates) would be required. The macro cell library as distributed uses five grids for the simple two input combinatorial gates. Since metal pitch generally lags behind silicon feature size, use of the minimum possible three grid wide cells would perhaps be more realistic. This change usually reduces required gate count by around ten percent (see tables 1 and 3). Of course, the space may need to be added back in the form of feed through cells.

2.2 Circuit Description

There are currently two primary bench mark circuits. The primary1 circuit is a medium size peripheral interface chip with 752 internal cells requiring 2673 gates, 904 signal nets, and 81 I/O pads [19]. At least one such chip is used on nearly every peripheral controller board. It has 32 input pads, 33 output pads, and 16 bidirectional pads. Internal nets contain 2785 total terminals with on average 3.08 per net. Internal cells have on average 3.70 terminals. The above values count master slice core area macro cell terminals but not I/O pad terminals. 255 terminals are unconnected, 30 cell inputs and 225 cell outputs, with 0.34 on average per cell. See table 1 for primary1 macro

cell usage by cell type and see table 2 for the net size profile.

The larger primary2 bench mark circuit is "a 16-bit microprocessor. It includes a sizeable register stack and some large pieces of decode logic" [19]. It has 2907 internal cells requiring 7600 gates, 3029 signal nets, and 107 I/O pads. There are 40 input pads, 50 output pads, and 17 bidirectional pads. Computer CPU boards that use commodity micro processors usually have a circuit similar to this one for glue logic. Internal nets contain 11000 terminals with on average 3.63 per net. Internal cells have on average 3.78 terminals per cell. 643 terminals are unconnected, 47 cell inputs and 596 cell outputs, with on average 0.22 per cell. See table 3 for macro cell usage and table 4 for the net size profile. The primary1 circuit has turned out to be rather easy to layout but is still of interest. The primary2 circuit has proven difficult and progress is still occurring [9].

3. Science in the Bench Mark Experimental System

3.1 Relation to Scientific Methodology

It is possible to perform experiments in the bench mark system that previous work in the methodology of science has identified as having importance for scientific growth. The most widely known condition first identified by Professor Kuhn requires the ability to solve puzzles [10]. There must be a way to decide within one approach (sometimes called a research program) if one technique is superior to another. For example, it should be possible to decide by scientific experiment within the simulated annealing research program if one annealing temperature schedule is superior to another. This requires the ability to control every possible variable and is possible in the bench mark experimental system. Of course, in an area dealing with human design, a possible experimental result might be that one method is better for one design or substrate type while another is better for another. The bench mark system may provide the capability to systematically characterize such differences. This last sort of puzzle solving is known as problem shifting or problem splitting [8].

Another condition first identified by professor Popper is the ability to falsify hypotheses (see [13] [8]). As a trivial example, without a controlled and widely available layout environment, it is impossible to falsify random placement. Imagine a claim of discovery that random placement with no evaluation function is superior to all other techniques. Without a controlled experimental system, the advocate of random placement could reasonably claim any falsification based on another implementation of random placement simply uncovered flaws in the implementation.

3.2 Problem with the Current Methodology

It is currently difficult to perform scientific experiments in the layout area. Papers reporting a new algorithm often have the following organization (see the table of contents and layout papers in a recent Design Automation Conference or ICCAD proceedings). A paper usually has the phrase "An algorithm to" in its title. Various problems with current approaches are identified. A new algorithm is presented. F1nally, a results section is presented that compares the new algorithm results to results from other algorithms or, in the case of on going research programs, to previous results achieved by a previous version of the same algorithm.

In this approach, it is impossible to determine whether comparisons use the same criteria. Even for comparisons between two algorithms within one system, it is often not possible to determine the exact reason for the improvements. Since layout systems are continually evolving, a factor other than the one described could be responsible for the improvement.

Scientific cooperation is impossible without shared assumptions and common coding schemes. It is difficult, for example, to combine one system's placement program with another system's router. The development of a commonly accepted measurement approach is not possible. Sometimes, program source code for an algorithm is supplied that is then modified to work within another system. If the algorithm works poorly in the new system, it is often not possible to isolate the reason. It could be a porting mistake, a hidden background factor that caused the algorithm to be specialized to the original layout system, or an algorithm problem.

3.3 Bench Mark Experiment Opportunities

The following types of experiments are possible within the layout bench mark experimental system.

1. Ability to directly compare different algorithms.
2. Ability to test substrate and master slice style properties.
3. Ability to analyze placements from other systems.
4. Ability to share algorithms that operate on the YAL data base.
5. Ability to criticize and improve the experimental bench mark system.
6. Ability to test approximations or heuristics with all factors but the one under test held constant.
7. Ability to systematically classify circuits.

3.4 Continuing Need for Careful Methodological Analysis

Even though the bench mark system offers significant possibilities, just the act of switching to the bench mark experimental system will not solve layout problems. Careful experimentation and analysis is still required. For example, the Physical Design work shops offered the opportunity to compare different placement algorithms by having them all routed by the UTMC router [15]. Even with all routing quality variability removed, problems arose that made objective evaluation difficult [16]. The UTMC router happened to insert one grid wide feed through cells where needed. Some of the placements required this feature, but some were made worse. Some placements achieved small area but required more feed through than the UTMC router was able to add. Those placements would probably, but not definitely, require more area after feed through addition. Various placements used a substrate size dictated by I/O pad geometry. These placements required larger area than was required by those which ignored I/O pads. The area determined from the circumference needed for I/O pads was much larger than the area required by internal cells. See [7, p. 127] and [20, figure 5] for more recent comparison problems.

3.5 Third Metal Layer Substrate Evaluation Experiment

A number of experimental master slice ASIC circuits use a third metal layer (metal3). The most obvious use dedicates metal3 to long vertical cell row feed through wires (actually feed over) that connect pins on rows separated by a intervening cell rows. The connection pattern illustrated in figure 3 would use the third metal layer but the patterns shown in figures 1 and 2 would not. The advantage of dedicating metal3 to long vertical connections is that such wire cause no congestion in the regions they cross. The alternative of dedicating metal3 to horizontal wires suffers from the problem that the vias that connect metal1 and metal3 horizontal wires in, for example, channel jogs block scarce vertical meta12 feed through grids. There may be some better mixed direction metal3 use that is not considered here.

Known good bench mark circuit placements can be used to measure the possible benefit from dedicating metal3 to vertical wires. The results discussed here use placements made for two layer metal by the Timberwolf system [17] to see how much track and feed through reduction is possible with simple rewiring. The Timberwolf 17 row primary1and 23 row primary2 placements remain among the best bench mark circuit placements. The next step would possibly be to repeat this experiment using placements from a placer modified to maximize vertical wiring. But since maximizing vertical wiring causes an increase in real wire length, the rewiring scheme discussed here may actually show the limit of potential size reduction from the addition of a third metal layer. The following data measures YAL coded Timberwolf placements and uses a placement level routing estimate approach described in [11]. The routing estimate decomposes each net into pin pairs using the minimum spanning tree and then assumes the connection can be made with at most one via. This measurement scheme gives an optimistic estimate of the gain from a third metal layer since if extra vias are needed, the long metal3 wires will cause additional congestion.

Tables 5 and 6 compare the rewired vertical feed through numbers for the primary 1 and primary2 circuits to the original two metal layer wire requirement where the spanning tree pin pair decomposition used exact physical wire length rather than weighing to maximize vertical wires. For exact physical wire length, a wire that connects rows separated by two intervening wiring channels and one cell row (see figure 3) along one vertical grid is as distant as a pin connecting to another pin 60 grids (20 gates) distant along the same row (see figure 1). For the three metal layer vertical wire maximizing measurement, the spanning tree distance metric assumes that the same vertical connection is equivalent to a pin only six grids (two gates) distant. Further decrease in vertical wire cost leads to no increase in horizontal wiring and no channel height decrease at least for the benchmark circuits. Column two contains the required vertical feed through wire number for each row for the two layer metal case. Column three gives the percentage of available feed through used. Available means non blocked meta12 grids and assumes that no vertical feed through would be lost to congestion problems. To understand the meaning of column three, consider the most congested primary2 circuit row 17. The required 1039 feed through wires is 23.7 percent more than available because the 23 row placement row length is 1005 grids of which 165 are blocked by vertical intracell wiring or unconnected pins (only 14). The percentage used is 1039/840 or 123.7. A value of more than 100 percent means a possible feed through shortage that requires either

additional feed through cells that would lengthen every row or a better global routing approach. Column four gives the number of long vertical wires that could possibly be moved to metal3. Column five gives the percentage of metal3 feed throughs that would be used above each row if every possible wire were moved to metal3.

Since the primary1 circuit has available feed throughs, adding a third metal layer does not lead to much area reduction. Nearly two thirds of the available metal3 feed through grids go unused over most internal rows. Global routing that makes maximum use of metal3 would, at a minimum, reduce the number of required track from 226 to 209 or 7.5 percent [11] (see [9] for a different approach to counting tracks). The trade off is a 10.4 percent increase in total wire length. This assumes the bench mark system uses the same pitch for all metal layers. A better global router could reduce the required maximum channel density by moving wires into horizontal channel sections that have unused grids below the maximum channel requirement thereby reducing channel density peaks, but then the same router could probably also reduce peaks in the two layer metal case [9].

Table 6 shows the saving for the primary2 circuit. The advantage of a third metal layer for the primary2 circuit is potentially larger since there is a shortage of meta12 vertical feed through tracks (see table 6 column 3). It is possible that a global router that changes connecting pin pairs to reduce vertical feed through requirements by using wiring channel sections that are below maximum channel density could possibly route the rows with a shortage of feed throughs. If the improvement is not possible, a global routing that maximizes use of metal3 would, at a minimum, reduce horizontal routing channel tracks from 544 to 486 or 10.7 percent. The trade off is a 15.1 percent increase in total wire length. Column five shows that more than half of the available metal3 tracks are used over the central rows and also that around half meta12 feed through tracks now are unused. If the master slice row lengths really needs to be increased by the 199 grids that row 17 requires in the two metal layer case, addition of a third metal layer can reduce total area by 25 percent (1005/1204*486/544). Of course, the actual decision to add a third metal layer will be determined by manufacturing and electrical considerations.

4. Discussion

In addition to the open layout questions discussed above, some open puzzle solving type problems are associated with the master slice layout experimental system itself. Improved algorithms for calculating circuit area that would involve more consensus concerning exactly what should be counted are needed. The bench mark simplifications need to be validated. If it turns out that the results predicted by this simplified system are unachievable when the actual details of feed through assignment and channel routing are implemented, the system would need to be changed to include those details. The bench mark experimental system needs to be developed and improved. Only the two primary bench marks circuits use enough wire to be interesting. Other circuits are distributed with the bench mark package (test00 through test08), but they lack wiring complexity since they were converted from an earlier one layer metal technology. The addition of larger (at least 20,000 gate) circuits would allow testing of the belief that current techniques will scale up. Small (primary1 size) circuits with large wire requirements

would be interesting, since it might be possible to characterize them exactly. Even though the bench mark circuits were designed using hierarchy, cells and nets were renamed to remove that information. Addition of bench mark circuits with element names containing hierarchical information, would allow direct comparison of flattened versus hierarchical approaches. See [21] for a discussion of additional circuit information a hierarchical layout system would require. One possible long term goal of bench mark experimentation would be discovery of enough theoretical principles to allow a developer faced with a new integrated circuit organization to be able to use those principles as guides in selecting algorithmic approaches and in choosing macro cell and substrate designs.

5. References

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Tables and Figures

Type	How Many	Gate Size	Feed Thrus	Gates Used	% of Total
F22	7	4.67	6	32.67	1.22
F32	251	6.67	7	1673.33	62.61
F42	11	6.67	7	73.33	2.71
G11	89	1.00	1	89.00	3.33
G12	54	2.00	2	108.00	4.04
G21	142	1.67	2	236.67	8.86
g31	97	2.00	1	194.00	7.26
g41	73	2.33	1	170.33	6.37
g61	27	3.33	2	90.00	3.37
g81	1	5.33	4	5.33	0.20

Internal cells requie 2672.67 gates (1 gate is 3 wire grids).
Average cell uses 3.55 gates with largest 6.67 and smallest 1.00.
2585 available in-cell feeds thrus (32.24% of totalor 0.97 per gate).
19 (22.47%) possible I/O connecting seed cells using 466.67 gates (17.46%).

TABLE 1. Primary1 Macro Cell Usage

Terminals in Net	Number of Nets	Terminals in Net	Number of Nets
2	477	10	1
3	249	11	6
4	67	12	9
5	24	13	1
6	28	14	3
7	13	16	1
8	2	17	11
9	9	18	3

TABLE 2. Primary1 Net Size Histogram

Type	How Many	Gate Size	Feed Thrus	Gates Used	% of Total
F22	550	4.67	6	2566.67	33.77
F32	39	6.67	7	260.00	3.42
F42	14	6.67	7	93.3	1.23
G11	367	1.00	1	367.00	4.83
G12	57	2.00	2	114.00	1.50
G21	715	1.67	2	1191.67	15.68
g31	437	2.00	1	874.00	11.50
g41	398	2.33	1	928.67	12.22
g61	278	3.33	2	926.67	12.19
g81	52	5.33	4	277.33	3.65

Internal cells requie 7599.33 gates (1 gate is 3 wire grids).
Average cell uses 2.61 gates with largest 6.67 and smallest 1.00.
7181 available in-cell feeds thrus (31.50% of totalor 0.94 per gate).
282 (9.70%) possible I/O connecting seed cells using 858.33 gates (11.29%).

TABLE 3. Primary2 Macro Cell Usage

Terminals in Net	Number of Nets	Terminals in Net	Number of Nets
2	1834	15	2
3	365	16	2
4	204	17	72
5	192	18	1
6	118	23	1
7	54	26	1
8	14	29	1
9	82	30	1
10	15	31	1
11	34	33	14
12	6	34	1
13	3	37	1
14	10		

TABLE 4. Primary2 Net Size Histogram

	Real Wire Distance		Two Rows Equal Two Gates	
Cell Row	Total Crossing Wires	% of Metal2 if no Metal3	Possible Metal3 Wires	%s of Metal3
1	188	57.7	33	6.9
2	243	73.3	48	10.1
3	223	70.8	68	14.1
4	286	85.5	120	25.1
5	279	84.3	144	29.9
6	283	83.4	177	36.9
7	291	88.2	195	40.5
8	324	94.1	208	43.2
9	334	95.7	192	40.0
10	307	89.7	176	36.6
11	324	94.2	153	31.8
12	284	86.3	137	28.5
13	263	82.1	119	24.8
14	252	77.2	102	21.3
15	246	74.7	78	16.2
16	227	68.8	50	10.4
17	220	67.9	24	5.0

TABLE 5. Primary1 Metal3 Vertical Feed Through Wires

	Real Wire Distance		Two Rows Equal Two Gates	
Cell Row	Total Crossing Wires	% of Metal2 if no Metal3	Possible Metal3 Wires	%s of Metal3
1	478	63.9	128	12.8
2	633	79.4	221	22.0
3	715	90.2	297	29.5
4	700	88.0	346	34.4
5	802	97.4	408	40.6
6	833	100.7	430	42.7
7	938	110.5	448	44.5
8	896	107.2	500	49.8
9	923	91.7	520	51.7
10	890	107.4	535	53.2
11	858	105.0	583	58.0
12	839	104.6	560	55.7
13	953	117.0	574	57.1
14	901	108.6	558	55.5
15	944	113.7	537	53.4
16	983	116.5	553	55.0
17	1039	123.7	566	56.3
18	1008	117.2	576	57.3
19	929	109.5	535	53.2
20	847	102.1	445	44.2
21	821	97.5	359	35.7
22	755	91.8	208	20.7
23	549	74.8	94	9.4

TABLE 6. Primary2 Metal3 Vertical Feed Through Wires

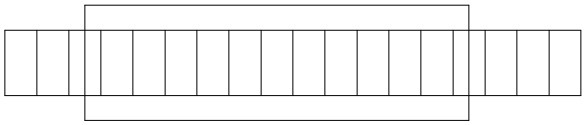

Figure 1. Along Channel Possible Connections

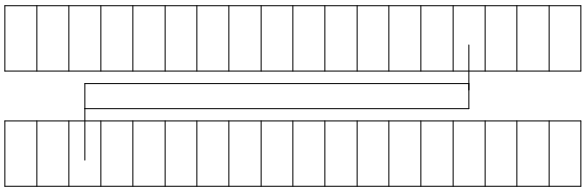

Figure 2. Cross Channel Connection

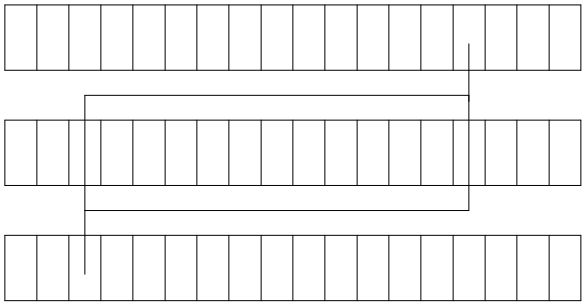

Figure 3. Cross Row One Via Possible Connections