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- ☐ White

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Black or African American. A person having origins in any of the black racial groups of Africa.
Native Hawaiian or Other Pacific Islander. A person having origins in any of the original peoples of Hawaii, Guam, Samoa, or other Pacific Islands.
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List of Suggested Reviewers or Reviewers Not To Include (optional)

SUGGESTED REVIEWERS:

Since this phase I research proposal involves both physics and computer science and proposes using a novel methodology, we would like to suggest some possible reviewers. In general, we believe that physicists will be able to objectively evaluate our proposal. Although he is emeritus, UC Berkeley Professor Frederick Reif will be familiar with methods involved in the original development of SPICE in the 1970s. Also, Carnegie Mellon University computer science professor James H. Morris was an assistant professor in the UC Berkeley L&S CS department who was not granted tenure but will understand the computer science part of our proposal. If non US reviewers are allowed, physics Professor Benny Lautrup of the Niels Bohr Institute in Copenhagen is familiar with the Niels Bohr methodology that we are using. Finally, Professor Arthur Fine of the University of Washington is an expert on the philosophy of physical problem solving.

REVIEWERS NOT TO INCLUDE:

Because Pragmatic C currently has a legal injunction involving one of our current products against Cadence Design Systems (refer to section A.7.3.4), we do not think that Cadence employees or consultants will be able to objectively evaluate our proposal. In particular, Professor Alberto Sangiovanni-Vincentelli, who is the author of one of the books we reference, should not be selected as a reviewer because he is a UC Berkeley EECS professor on leave as chief scientist of Cadence Design Systems.

COVER SHEET FOR PROPOSAL TO THE NATIONAL SCIENCE FOUNDATION

PROGRAM ANNOUNCEMENT/SOLICITATION NO./CLOSING DATE/if not in response to a program announcement/solicitation enter NSF 03-041

NSF 03-535 **06/12/03**

FOR CONSIDERATION BY NSF ORGANIZATION UNIT(S) (Indicate the most specific unit known, i.e. program, division, etc.)

DMI - SMALL BUSINESS PHASE I

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0340256

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NAME OF ORGANIZATION TO WHICH AWARD SHOULD BE MADE

Pragmatic C Software Corp.

AWARDEE ORGANIZATION CODE (IF KNOWN)

6250006893

ADDRESS OF AWARDEE ORGANIZATION, INCLUDING 9 DIGIT ZIP CODE

520 Marquette Ave
suite 900
Minneapolis, MN 55402-1122

NAME OF PERFORMING ORGANIZATION, IF DIFFERENT FROM ABOVE

PERFORMING ORGANIZATION CODE (IF KNOWN)

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☒ FOR-PROFIT ORGANIZATION ☐ WOMAN-OWNED BUSINESS

☐ IF THIS IS A PRELIMINARY PROPOSAL THEN CHECK HERE

TITLE OF PROPOSED PROJECT **SBIR/STTR Phase I: SPICE Circuit Simulator Direct Solution Improvement**

REQUESTED AMOUNT	PROPOSED DURATION (1-60 MONTHS)	REQUESTED STARTING DATE	SHOW RELATED PRELIMINARY PROPOSAL NO. IF APPLICABLE
$ **51,681**	**6** months	**09/01/03**	

CHECK APPROPRIATE BOX(ES) IF THIS PROPOSAL INCLUDES ANY OF THE ITEMS LISTED BELOW

☐ BEGINNING INVESTIGATOR (GPG I.A)
☐ DISCLOSURE OF LOBBYING ACTIVITIES (GPG II.C)
☐ PROPRIETARY & PRIVILEGED INFORMATION (GPG I.B, II.C.6)
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PI/PD DEPARTMENT
Computer Science

PI/PD FAX NUMBER
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PI/PD NAME **Steven J Meyer**	**MS**	**1972**	**612-371-2023**	**sjmeyer@pragmatic-c.com**
CO-PI/PD				
CO-PI/PD				
CO-PI/PD				
CO-PI/PD				

Electronic Signature

CERTIFICATION PAGE

Certification for Authorized Organizational Representative or Individual Applicant:

By signing and submitting this proposal, the individual applicant or the authorized official of the applicant institution is: (1) certifying that statements made herein are true and complete to the best of his/her knowledge; and (2) agreeing to accept the obligation to comply with NSF award terms and conditions if an award is made as a result of this application. Further, the applicant is hereby providing certifications regarding debarment and suspension, drug-free workplace, and lobbying activities (see below), as set forth in Grant Proposal Guide (GPG), NSF 03-041. Willful provision of false information in this application and its supporting documents or in reports required under an ensuing award is a criminal offense (U. S. Code, Title 18, Section 1001).

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(If answer "yes", please provide explanation.)

Is the organization or its principals presently debarred, suspended, proposed for debarment, declared ineligible, or voluntarily excluded from covered transactions by any Federal department or agency? Yes ☐ No ☒

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This certification is required for an award of a Federal contract, grant, or cooperative agreement exceeding $100,000 and for an award of a Federal loan or a commitment providing for the United States to insure or guarantee a loan exceeding $150,000.

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The undersigned certifies, to the best of his or her knowledge and belief, that:

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AUTHORIZED ORGANIZATIONAL REPRESENTATIVE	SIGNATURE	DATE
NAME **Steven J Meyer**	**Electronic Signature**	**Jun 12 2003 5:13PM**

TELEPHONE NUMBER	ELECTRONIC MAIL ADDRESS	FAX NUMBER
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NATIONAL SCIENCE FOUNDATION
Program Solicitation/Instruction Guide Number **NSF 03-535**

SBIR PHASE I - PROPOSAL COVER PAGE

TOPIC	SUBTOPIC LETTER (if any)	TOPIC TITLE
IT	**E1**	**Information-Based Technologies**

PROPOSAL TITLE **SBIR/STTR Phase I: SPICE Circuit Simulator Direct Solution Improvement**

COMPANY NAME	EMPLOYER IDENTIFICATION NUMBER (EIN) OR TAXPAYER IDENTIFICATION NUMBER (TIN)
Pragmatic C Software Corp.	**943124971**

NAME OF ANY AFFILIATED COMPANIES (Parent, Subsidiary, Predecessor)

ADDRESS (Including address of Company Headquarters and zip code plus four digit extension)
520 Marquette Ave
suite 900
Minneapolis, MN 55402-1122

REQUESTED AMOUNT	PROPOSED DURATION	PERIOD OF PERFORMANCE
$51681	**6**	

THE SMALL BUSINESS CERTIFIES THAT:	**Y/N**
1. It is a small business as defined in the solicitation.	**Y**
2. It qualifies as a socially and economically disadvantaged business as defined in the solicitation. (FOR STATISTICAL PURPOSES ONLY.)	**N**
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4. NSF is the only Federal agency that has received this proposal (or overlapping or equivalent proposal) from the small business concern. If No, you must disclose overlapping or equivalent proposals and awards as required by this solicitation.	**Y**
5.SBIR: A minimum of two-thirds of the research will be performed by this firm in Phase I. STTR: It will perform at least 40 percent of the work and the collaborating research institution will perform at least 30 percent of the work as described in the proposal.	**Y**
6. The primary employment of the Principal Investigator will be with this firm at the time of the award and during the conduct of the research.	**Y**
7. It will permit the government to disclose the title and technical abstact page, plus the name, address and telephone number of a corporate official if the proposal does not result in an award to parties that may be interested in contacting the small business for further information or possible investment.	**Y**
8. It will comply with the provisions of the Civil Rights Act of 1964 (P.L. 88-352) and the regulations pursuant thereto.	**Y**
9. It has previously submitted proposals to NSF.	**N**
10. It previously submitted this proposal (which was declined) and significant modifications have been made as described in the solicitation.	**N**
11. It has received Phase II awards from the Federal Government. If "yes" provide a company commercialization history in the supplementary documents module.	**N**

PRINCIPAL INVESTIGATOR / PROJECT DIRECTOR

NAME **Steven J Meyer**

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612-371-2023	**612-349-5230**	

COMPANY OFFICER (FOR BUSINESS AND FINANCIAL MATTERS)

NAME	TITLE	TELEPHONE NO.
Steven J Meyer	**President**	**612-371-2023**

OTHER INFORMATION

PRESIDENTS NAME **Steven J Meyer** YEAR FIRM FOUNDED **1989**

NUMBER OF EMPLOYEES (including Parent, Subsidiary, Predecessor)
AVERAGE PREVIOUS 12 MO.: **2** CURRENTLY: **2**

RESEARCH INSTITUTION NAME
Pragmatic C Software Corp.

RESEARCH INVESTIGATOR NAME

RESEARCH INVESTIGATOR TELEPHONE NO.

PROPRIETARY NOTICE: See instructions concerning proprietary information.
Check Here ☐ if proposal contains proprietary information.

A.7.2 Project Summary

Intellectual Merit

This Small Business Innovation Research (SBIR) Phase I project will demonstrate the feasibility of, and develop prototype computer code for, increasing the speed and capacity of the SPICE circuit simulation computer program. SPICE works by directly solving the differential equations that describe circuit transistors. Exact equation solution is extremely accurate but capacity limited. SPICE is the circuit simulation tool of choice because other approaches are inaccurate or unstable but SPICE usage is limited because it is too slow and uses too much memory. Therefore, SPICE capacity improvement has immediate and wide spread value in solving the circuit verification problem.

To establish the feasibility of increasing SPICE capacity, the direct equation solving SPICE computer code will be rewritten by first separating out the circuit physics from the computer implementation to show the relationship between the computer implementation and the underlying electrodynamics. Next, physical characterizations developed by the founders of modern physics will be studied and applied to improve SPICE equation solving. The new prototype computer code will then be evaluated and measured using commercial circuits in order to develop better characterizations and even better direct solution computer code.

Broader Impacts of the Study

The SPICE circuit simulation system is the de facto analog circuit verification standard so any improvement in SPICE will be of immediate value to every company that develops electronics. SPICE direct solution capacity improvement will enhance the productivity of circuit designers. In addition, by using the natural philosophy scientific method that led to the growth of modern physics, scientific progress in areas that combine physics and computation will be facilitated. The applicant plans to commercialize the technology by licensing either computer code or technology.

Keywords: SPICE, Analog Verificition, Circuit Simulation, Direct Solution Method

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For font size and page formatting specifications, see GPG section II.C.

*Proposers may select any numbering mechanism for the proposal. The entire proposal however, must be paginated. Complete both columns only if the proposal is numbered consecutively.

SPICE Circuit Simulator Direct Solution Improvement

A.7.3 Project Description

A.7.3.1 Identification and Significance of the Innovation

Electronic systems are an important and growing part of the world economy. Integrated circuits (ICs) are now so complex that design and verification is impossible without use of Ecad software. The increasing popularity of communication and consumer electronic systems has increased the need for verification of analog and mixed signal circuits. Mixed signal ICs contain both digital and analog components. Design and verification of the digital part of mixed signal circuits is well understood, but little progress has been made in the area of analog design and verification. Kundert[2000] is a good introductory paper discussing analog and mixed signal design problems.

Analog verification using circuit simulation is the main analog verification method. The SPICE circuit simulation system (Nagel[1975]) was developed in the mid 1970s and remains, to this day, the most popular analog circuit verification method. SPICE works by first converting circuit transistors and transistor interconnections to a set of ordinary differential equations and then exactly solves those equations using numerical methods. Although SPICE solves the analog simulation problem, it is too slow and uses too much computer memory to simulate modern large circuits.

A number of research projects have attempted to solve the analog circuit simulation capacity problem, but in spite of claims of imminent success during the 1980s, all circuit simulation improvements are heuristic in the sense that they either show inconsistent capacity improvement (better than SPICE for some circuits, worse for others) or sacrifice accuracy. Sacrifice of accuracy is particularly problematic because it misses catastrophic circuit failures and instabilities and adds oscillations that do not occur in the physical circuit. Heuristic methods also suffer from the problem that they are MOS transistor specific.

During the 1980s so called third generation circuit simulation methods that replaced exact solution of electrodynamic differential equations with approximations were proposed. The most prominent method was called relaxation (Sangiovanni[1987] for example). However, the third generation methods were not popular with circuit designers because they lacked accuracy. During the 1990s, the goal of circuit simulation improvement using approximate methods was abandoned. Instead, methods that approximated circuit elements using some kind of lumped circuit description but were much faster than SPICE were studied (Shih[1991] and Lewis[1992]). The most popular commercial method is called hierarchical simulation because it allows an entire IC to be approximately

simulated. This method works by evaluating interactions between simplified lumped (capacitive) models (Koh[1999] discloses commercial realization of this idea).

During the current decade, the superiority of original SPICE has been acknowledged. Research has split into two areas. One area abandons accurate circuit simulation and replaces circuit simulation with symbolic switch level timing simulation (McDonald[2001] for example). Another approach attempts to augment SPICE to allow simulation of newer circuit element types (Bhattacharya[2001] for example) or to use accurate SPICE simulation as components of other programs (Phelps[2000] for example). SPICE remains the analog circuit simulation method of choice and the market for SPICE simulation is extremely large because every company that designs electronics uses it.

Accurate SPICE simulation of large analog circuits remains the most important unsolved circuit verification problem. SPICE improvement has immediate economic value because SPICE is the de facto "gold" standard for circuit simulation. SPICE development was financed by US Government research grants and is available under BSD software license so there are no intellectual property (IP) impediments to achieving commercial success from improvements. SPICE simulation runs often take hours and capacity is limited to at most a few thousand transistors in spite of the ten or more fold computer speed improvements during the last decade. The SPICE capacity problem has also limited automation of analog circuit design and verification. A speaker at a recent Design Automation Conference panel called analog design and verification "pre-scientific magic" because analog verification requires designers to verify large analog ICs from a few SPICE runs of only small subcircuits. Finally, analog synthesis is impossible because accurate SPICE simulation is too slow to allow figure of merit searching of circuit design parameters.

A.7.3.2 Background and Phase I Technical Objectives

The proposed phase I program is directed at demonstrating the feasibility of significant speed and capacity improvement to the SPICE electrical circuit equation solving computer code by improving the direct solution method. The direct solution method has a number of advantages: 1) it is accurate and stable, 2) it does not depend on the properties of MOS circuits, and 3) no instabilities and oscillations are introduced by the simulation algorithm.

Approaches to SPICE circuit simulation speed improvement can conveniently be divided into three categories: 1) direct solution methods, 2) heuristic solution methods such as relaxation, and 3) hierarchical circuit decomposition methods. Designers do not trust approaches 2) and 3) but are forced to utilize Ecad tools that use those methods because direct solutions method

are capacity limited. Development of a fast direction solution circuit simulation would have large commercial value.

So far, direct solution research has been aimed at analyzing and improving speed of SPICE by improving only the Newton-Raphson integration algorithm (Yu[1989], Eickhoff[1995] and Ngoya[1997]). All proposed changes are heuristic in the sense that speed improvements depend on "equation ordering".

It is believed that significant progress is possible in the direct solution method using the scientific method developed as part of early twentieth physics which studied physics as natural philosophy. This approach allows circuit physics and computational algorithm to be studied and improved independently. We believe that the founders of modern physics solved problems that can be applied to improve the direct solution method when implemented on modern computers.

The algorithms will then be further developed, implemented and optimized for commercial size circuits during phase II research. Such an improvement will have large additional economic benefit because it would allow use of analog circuit verification techniques that are currently impossible. Phelps[2000] discusses one such tool that would be significantly better if faster SPICE direction solution method simulation were possible.

A.7.3.2.1 Our Novel Methodological Approach

After World War II and up to the period when SPICE was developed, semiconductor circuit behavior was studied as physics within the natural philosophy framework rather than engineering. Engineering disciplines do not use the scientific method and are limited to computational methods developed outside of engineering. Professor William Shockley, who invented the transistor, insisted on separating himself from engineering and instead worked with theoretical physicists at Stanford University. This decision leads us to believe that reexamination of the direct solution circuit simulation method in terms of the development of the physics of electrodynamics has promise. Also, physicists during the early 1970s imagined new physical problem solving methods involving computer science. One can see some of this anticipation of improved physical computation in Schiff's quantum mechanics text book (Schiff[1955]) and in the Felix Bloch interview in the Archive for Quantum Physics (AHQP). Another way of understanding the lack of circuit simulation progress is that current algorithms use computers to implement only pre-computer era algorithms.

There is also some evidence going back to the end of the 19th century at Humboldt University in Berlin that physicists such as Kirchoff and Planck, who followed Kirchoff in the chair of natural philosophy, intentionally avoided Newtonian computational methods. Unfortunately, since the Planck papers were lost during the 1930s, the only evidence of this is correspondence between

Professor Runge (who taught at Tuebingen at the time) and Planck. The letters are available at the Max Planck Archive of the Kaiser Wilhelm Institute in Berlin. This may be significant because all current circuit simulation algorithms assume the use of Newton-Raphson integration.

Another reason to believe that progress is possible arises from the current EECS (electrical engineering and computer science) methodology in which engineering is viewed as mathematical formalism. This contrasts with the experimental and critical thinking that dominated physics when SPICE was first developed. The following quotation from Niels Bohr (Bohr[1987], p. 550) from his 1954 lecture "Mathematics and Natural Philosophy" presented at New York University can be interpreted as specific directions for improving electrodynamic calculations.

> The general lesson of the role that mathematics has played through the ages in natural philosophy is the recognition that no relationship can be defined without a logical frame and that any apparent disharmony in the description of experience can be eliminated only by an appropriate widening of the conceptual framework. This lesson, familiar to mathematicians, and conspicuous in studies in the foundations of their science, has been enforced by the development of physics in a way that has a bearing on many other fields of human knowledge and interest in which we met with similar situations in the analysis and synthesis of experience.

To understand the limitations of the current formalist view, contrast Bohr's quotation with Professor Knuth's formalist view quoted in Nielsen[2001], p. 171 that computation algorithms must be proven and, although this is not explicitly stated in quotation, that algorithm improvements must come from analysis of the mathematical proof of algorithm efficiency.

> Like mathematics, computer science will be somewhat different from the other sciences, in that it deals with artificial laws that can be proved, instead of natural laws that are never known with certainty.

A.7.3.3 Phase I Technical Objectives

The overall goal of this program is to first demonstrate the feasibility of, and then to develop prototype computer code for, a fast SPICE direct solution solver. Our goal is to develop a method which is at least 10 times faster than current SPICE direct solver with the properties that it is not MOS circuit specific, that it does not depend on equation order or other heuristics and that it is as accurate as current SPICE.

In pursuit of this goal, we will address the following technical questions:

1. Can SPICE direct solution be improved by separating out physics from computer science algorithm implementation?
2. What is the relationship in SPICE circuit simulation between physical electrodynamics of circuits and numerical computer implementation methods?
3. Determine if there are any legacy transistor models and circuit conventions that prevent commercial use of an improved direct solver?
4. Are there any patterns or other information that can be learned from systematic measurement of commercial SPICE circuit simulation performance?
5. Were any discoveries made by the founders of modern physics that can be utilized in circuit simulation?

The tasks necessary to answer the above questions are detailed in the next section.

A.7.3.4 Phase I Research Plan

Task 1 - Set up SPICE 3f5 development environment and locate commercial test circuits

The beginning of the project involves setting up a program to develop an environment for rewriting part of SPICE 3f5. The task involves determining inter-relationships between source files and either finding or developing methods for tracing calculation steps and for quickly debugging problems. The task also involves developing methodology for measuring performance that is repeatable and isolates specific problem areas.

Further more, part of this task involves locating commercial bench mark circuits because nearly all the academic papers use only a few stylized benchmark circuits. Pragmatic C may need to sign non disclosure agreements (NDAs) to gain access to such commercial circuits. Pragmatic C has extensive industrial contacts because its Verilog simulator was licensed as the digital engine for a mixed signal (analog and digital) simulator.

Task 2 - Rewrite direct solver code to separate out the physics

The current SPICE direct solver code implements the solver by calling standard computational subroutines from numerical analysis. The original SPICE code was developed when only a few numerical subroutines were available so the numeric calculations dictated the physical representations. In other words, pre-

computer physical representations were expressed using whatever numeric subroutines happened to be available. By rewriting and simplifying direct solver code, hopefully physical representations and algorithms can be matched to improve solver speed and reduce memory usage. One possible problem with current SPICE solver implementations is that the underlying physics and the numeric algorithm are difficult to separate. Task 2 is feasible in a PHASE I six month project because there are only about 10K lines of C source code involved.

Task 3 - Determine if old modern physics discoveries can be applied

There are a number of promising areas that require going back to study historical results during the development of modern physics. Much of that development was limited by calculation speed and anticipated the development of digital computers. One promising area involves studying the original papers by Kirchoff and Runge to see if they discovered better electro-physical methods that have been lost over time. A related historical source that may contain discussions of physical discoveries that can be applied to direct solution method is the Archive for Quantum Physics (AHQP). It has interviews with and unpublished material by the founders of modern physics. At Stanford and at SLAC, many computer scientists were invited to visit because those founders of modern physics imagined our current computerized world.

The Univerity of Minnesota has both the AHQP archive and an extensive collection of physics periodicals from the late 19th and early 20th centuries. Finally, computation methods used in cryptography may offer methods for improving SPICE direct solution methods. In particular, the methods used in inverting matrices as part of prime number factorization may be applicable (for example Lenstra[1987] and Lenstra[1992]).

Task 4 - Use results of task 2 and task 3 to develop prototype code

After completing tasks 2 and 3, the SPICE direct solver code will be rewritten to achieve the speed and memory utilization improvements.

Task 5 - Set up measurement system and take measurements

A repeatable and automated measurement system is required for phase II commercial algorithm development and debugging. It will also allow publication of measurements which may assist other scientific circuit verification research.

Task 6 - Determine if new algorithms are inter-operable

By running SPICE re-implementation with separated out physics and also running current SPICE 3f5, determine if new algorithms can mimic results expected by commercial electronic analog design flows. Locate any transistor model or processing order dependencies. It will be known at the end of this stage

if legacy transistor model and circuit design properties limit the types of direction solution algorithm changes that are usable in current commercial design flows. If there are such barriers, we will attempt to develop direct solution methods that remain inter-operable.

Task 7 - Preliminary commercialization analysis and preparation of final report

In this task we will make use of data obtained in Tasks 2, 3, 5 and 7 to perform technical evaluation. These evaluations will determine the feasibility of the technology and the feasibility of proceeding with submission of a Phase II proposal. The results will appear in our final report. Since Pragmatic C intends to license technology or software, licensees will be responsible for phase III commercialization.

The approximate time line for the proposed research requires one month for Task 1. One month for Task 2. Then the main research effort of discovering the faster direct solution algorithm that will take 3 months. Task 5 will overlap tasks 2 and 3. Tasks 6 and 7 plus further develop of the new algorithm will occur during the last month of the project. Although, if possible, preliminary inter-operability determination will start earlier than the last month.

A.7.3.4 Company Information

Pragmatic C Software was started in 1989 in California and moved to Minnesota in 2000. It developed software with high mathematical content that is sublicensed.

The First product from Pragmatic C was the Vcmp net list translator that allowed digital circuits entered using the Valid Logic Scald schematic editor to be simulated using Verilog. Before Vcmp, the translation process from proprietary workstation hardware internal circuit net list into Verilog required hours of computer time. Vcmp reduced translation time to seconds for medium size circuits and to minutes for million gate circuits. Vcmp was originally developed by the proposed principle investigator. The net list discovery is described in Meyer[1988]. Vcmp was sublicensed to a Massachusetts company Gateway Design Automation in exchange for per copy royalties. Vcmp intellectual property was protected using Copyright and a sublicensing contract. Gateway was then purchased by Cadence Design Systems. Cadence Design refused to pay the contractual royalties. The dispute was arbitrated and Pragmatic C finally prevailed in 1997 and was awarded $1.6 million in damages. Cadence Design was eventually able to reverse engineer Vcmp functionality as part of their integrated design environment but only after years of effort.

Once it became clear that Cadence Design was going to try to give away

Vcmp without paying royalties, it became clear that reverse engineering Vcmp was not difficult enough. Pragmatic C then started developing a Verilog digital circuit simulator. The simulator called Cver was first used as the original front end elaborator during development of the VCS simulator by a small company named Chronologic. Chronologic was later purchased first by View Logic and then View Logic was purchased by Synopsys Corporation.

In 1998 a venture capital financed startup Antrim Design Systems of Scotts Valley California licensed Cver as the digital engine for their planned Verilog-AMS simulator (analog mixed signal). After evaluating the two digital Verilog simulators developed by OEM companies. Antrim selected Cver and signed a licensing agreement to link Cver-ams object code as the digital solver for their planned Verilog-AMS mixed signal simulator.

Pragmatic C proposed extending Cver to read and elaborate Verilog-AMS HDL and to connect the Cver digital simulation engine with the Antrim SPICE Analog simulation engine using the IEEE P1364 standardized application programming interface called vpi_ PLI 2.0 interface. The development project was successful and Antrim Verilog-AMS product called ams started shipping in 1999. During the high tech downturn in late 2001 and early 2002, Antrim sales fell and in late 2002 Antrim Design assets were sold to Cadence Design Systems. At the time of sale, Antrim owed a considerable amount of money to Pragmatic C. Antrim recently agreed to pay Pragmatic C to settle the federal court Copyright case (ref. United States Federal Court Minnesota, Third Division, file No. CV-02-2502). The preliminary injunction granted to Pragmatic C preventing Antrim Design Systems from transferring Pragmatic C code to Cadence Design Systems has been made permanent.

A.7.3.5 Commercial Potential

Since SPICE input and Berkeley SPICE 3f5 are the de facto industry standard, any improvements will immediately have commercial value. Because the project aims at direct solution approach improvement, any new algorithms will be immediately popular with designers because they will not need to deal with instabilities and other accuracy problems.

SPICE source code was developed under US government research grants and therefore is publicly available and licensed under the BSD software license that allows SPICE with improved equation solving code to be sold commercially. SPICE 3f5 is a small program. The SPICE 3f5 source directory is only about 8 MB and the integration and sparse matrix solver source code is only 11 thousand lines of C source (the included header files add a few thousand more lines). Therefore, a small company can feasibly focus on just improving the direct solver part of the SPICE program. Any improvements can immediately be utilized by

large electronic or Ecad companies and the changes immediately fit into analog electronic design flows. Ecad tools that fit into analog design flows must accept SPICE circuit description input or they will not be used.

There are commercial SPICE simulators on the market but those programs mostly add convenient user interfaces and better and more comprehensive device models such as BSIM3. Except for a few cases, the commercial SPICE additions will work with any improved direct solver. Commercial SPICE simulators and Berkeley SPICE 3f5 can be used interchangeably because most large electronic companies continue to run Berkeley version 3f5 SPICE as part of their design flow. Therefore, any future extensions must remain compatible with 3f5.

Since Pragmatic C intends to remain a small R&D company, the best opportunity for commercialization would be to license software code in object form that can be linked with normal SPICE 3f5. Such linking is allowed because SPICE 3f5 is distributed under the BSD software license. Another possibility would be to license the technology discovered during this research project to a company that would combine it with their technology. A third possibility would be to license SPICE with improved direct solver to a company that markets and supports Ecad tools. A fourth possibility would be to obtain commercial R&D contracts with electronic companies who would benefit from the improved SPICE in developing non MOS electronic devices such as magneto-resistive memories. Many small companies are trying to break into the Ecad software market but have trouble succeeding. There would be large economic advantage to partner with a company that has developed advanced technology.

A.7.3.5.1 Interoperability - Important Commercialization Issue

Since every electronic design company uses SPICE many conventions and legacy circuit designs have accumulated. If commercial transistor models and legacy circuits depend on accidental properties of current 3f5 or commercial SPICE solvers to such an extent that no algorithm changes are possible, this will somewhat limit the commercial market size of direct solver improvements. An important objective of the Phase I research project is to determine any interoperability problems, but even if this interoperability problem is so serious that current algorithms must be exactly mimicked, there are still many commercial opportunities. For example, vertically integrated companies who develop their own transistor and process models, will still be able to use SPICE with new solver.

For example, Pragmatic C encountered an example of an interoperability problem while developing Cver. Cver implements the switch level algorithm implemented by the original digital Verilog simulator called Verilog XL from Cadence. The Verilog XL algorithm is close to the algorithm described in Bryant[1984] but modified so that digital loads and drivers can interact with the

switch channel relaxation algorithm. It turns out that because customer design fbws rely on various implementation assumptions such as evaluation order of the original XL algorithm, speed improvement is diffi cult.

A.7.3.6 Consultants and Subawards/Subcontractors

No consultants are presently foreseen for the Phase I program. If a need should arise, mathematicians or physicists from University of Minnesota or other Midwestern universities will be utilized.

A.7.3.7 Equivalent or Overlapping Proposals to Other Federal Agencies

No work substantially similar to that proposed here is being conducted at this time, nor is any pending.

A.7.4 References Cited

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A.7.5 Biographical Sketches

Principal investigator Steven Meyer was educated at Stanford Univerity by the founders of modern physics at the end of their careers and has over 25 years research and development experience in computer science and Ecad software. Steven Meyer and Andrew Vanvick research and develop all algorithms and following natural philosophy physics tradition document their own algorithms and write their own computer code.

Steven Meyer has been president of Pragmatic C Software Corp. since its inception in 1989 after becoming an independent consultant in 1986. Pragmatic C Software has developed two complex software products that were sublicensed to small Ecad companies. In the 1980s, the Vcmp Valid Logic CAD System to Verilog HDL translator was developed and sublicensed to Gateway Design Automation that was purchased by Cadence Design Systems in 1990. The Vcmp program was based on discovery of a new method for representing net lists described in a Design Automation Conference paper (see Meyer[1988]) but because at that time software was not patentable, the method was not patented.

Then starting in 1992 Pragmatic C developed the Cver full IEEE P1364 standard Verilog digital HDL simulator. Cver was licensed to venture capital financed startup Antrim Design Systems as the digital engine for their Verilog-ams simulator until Antrim Design was purchased by Cadence Design Systems in November 2002. Full P1364 Verilog simulators are so difficult that only five simulators exist.

From 1982 to 1984 Steven Meyer was employed by LSI Logic corporation where he developed the first gate array (called logic array at the time) placement program. The algorithm and program are described in a paper presented at the 1983 ICCD conference (Meyer[1983]). This algorithm was the first use of minimum spanning trees in physical design and preceded the next use by nearly a decade. At LSI Logic, he next developed the computer programs for the first engineering workstation logic array design system. Prior to joining LSI Logic, Steven Meyer worked at Zilog Corporation where he wrote the PLZ compiler code generator for the Z80 microprocessor.

Andrew Vanvick graduated from Univerity of Minnesota in 2002 where he received a B.S. degree in computer science. He worked as an intern at Pragmatic C during summer of 2001 before his senior year. He is joint author of the paper "A Verilog HDL Virtual Machine".

Resume for Principal Investigator Steven Meyer

Education:

No Ph.D. but passed orals and wrote intended thesis (intended thesis available at http://www.pragmatic-c.com/docs/StructProgBook-IntendedThesis.pdf). After EE Department annexed computer science department in the school of literature and science, thesis was rejected and appeal to chancellors office was denied (appeal correspondence available upon request).

M.S., computer science, UC Berkeley, Berkeley, CA, 1972.

B.S., physical science individually designed major that included math, physics and computer science, Stanford Univerity, 1970. Won Freshman honors calculus best final score award.

Publications

Meyer[1978] Meyer, S. A failure of structured programming. Zilog Corporation Technical Report No. 5, Zilog Corporation, 1978 (available on web as chapter 1 of intended. Ph.d. thesis url http://www.pragmatic-c.com/docs/StructProgBook-IntendedThesis.pdf).

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Meyer[2003] Meyer, S. and Vanvick, A. Verilog HDL virtual machine. (available at http://www.pragmatic-c.com/docs/ver-vm.pdf). In preparation, 2003.

Meyer[2003b] Meyer, S. Cryptography, CS, and quantum computing research program testing. Slides and sceptical side annotated bibliography from rump session talk given at Eurocrypt 2003 in Warsaw Poland, 2003 (available at http://www.pragmatic-c.com/docs/QuantCompSceptical.pdf).

Pending Patent Applications (both published)

US0138244A1 Priority date 09/1999, Simulator Independent Object Code HDL Simulation using PLI.

US0049576A1 Priority Date 07/2000, Digital and Analog Mixed Signal Simulation Using PLI API (also published as WO0203310A1 Mixed Signal Simulation).

Resume for Andrew Vanvick

Education:

Taking classes at University of Minnesota toward graduate degree.

B.S., computer science, Univerity of Minnesota, Minneapolis, MN, 2002.

Publications

Meyer[2003] Meyer, S. and Vanvick, A. Verilog HDL virtual machine. (available at http://www.pragmatic-c.com/docs/ver-vm.pdf). In preparation, 2003.

SUMMARY PROPOSAL BUDGET YEAR 1

FOR NSF USE ONLY		
PROPOSAL NO.	DURATION (months) Proposed	Granted
AWARD NO.		

ORGANIZATION
Pragmatic C Software Corp.

PRINCIPAL INVESTIGATOR / PROJECT DIRECTOR
Steven J Meyer

A. SENIOR PERSONNEL: PI/PD, Co-PI's, Faculty and Other Senior Associates (List each separately with title, A.7. show number in brackets)	NSF Funded Person-months CAL	ACAD	SUMR	Funds Requested By proposer	Funds granted by NSF (if different)
1. **Steven J Meyer - president**	2.40	0.00	0.00	$ 18,720	$
2. **Andrew I Vanvick - technical staff**	3.40	0.00	0.00	12,600	
3.					
4.					
5.					
6. (0) OTHERS (LIST INDIVIDUALLY ON BUDGET JUSTIFICATION PAGE)	0.00	0.00	0.00	0	
7. (2) TOTAL SENIOR PERSONNEL (1 - 6)	5.80	0.00	0.00	31,320	
B. OTHER PERSONNEL (SHOW NUMBERS IN BRACKETS)					
1. (0) POST DOCTORAL ASSOCIATES	0.00	0.00	0.00	0	
2. (0) OTHER PROFESSIONALS (TECHNICIAN, PROGRAMMER, ETC.)	0.00	0.00	0.00	0	
3. (3) GRADUATE STUDENTS				8,420	
4. (0) UNDERGRADUATE STUDENTS				0	
5. (0) SECRETARIAL - CLERICAL (IF CHARGED DIRECTLY)				0	
6. (0) OTHER				0	
TOTAL SALARIES AND WAGES (A + B)				39,740	
C. FRINGE BENEFITS (IF CHARGED AS DIRECT COSTS)				0	
TOTAL SALARIES, WAGES AND FRINGE BENEFITS (A + B + C)				39,740	
D. EQUIPMENT (LIST ITEM AND DOLLAR AMOUNT FOR EACH ITEM EXCEEDING $5,000.)					
TOTAL EQUIPMENT				0	
E. TRAVEL 1. DOMESTIC (INCL. CANADA, MEXICO AND U.S. POSSESSIONS)				1,480	
2. FOREIGN				0	
F. PARTICIPANT SUPPORT COSTS					
1. STIPENDS $ 0					
2. TRAVEL 0					
3. SUBSISTENCE 0					
4. OTHER 0					
(0) TOTAL PARTICIPANT COSTS				0	
G. OTHER DIRECT COSTS					
1. MATERIALS AND SUPPLIES				1,080	
2. PUBLICATION COSTS/DOCUMENTATION/DISSEMINATION				0	
3. CONSULTANT SERVICES				0	
4. COMPUTER SERVICES				0	
5. SUBAWARDS				0	
6. OTHER				6,000	
TOTAL OTHER DIRECT COSTS				7,080	
H. TOTAL DIRECT COSTS (A THROUGH G)				48,300	
I. INDIRECT COSTS (F&A)(SPECIFY RATE AND BASE) **(Rate: , Base:)**					
TOTAL INDIRECT COSTS (F&A)				0	
J. TOTAL DIRECT AND INDIRECT COSTS (H + I)				48,300	
K. FEE (IF REQUESTED MAXIMUM = 7% OF J)				3,381	
L. TOTAL COST AND FEE (J + K)				$ 51,681	$

PI/PD NAME
Steven J Meyer

ORG. REP. NAME*
Steven meyer

FOR NSF USE ONLY		
INDIRECT COST RATE VERIFICATION		
Date Checked	Date Of Rate Sheet	Initials - ORG

 ***ELECTRONIC SIGNATURES REQUIRED ONLY FOR REVISED BUDGET**

SUMMARY PROPOSAL BUDGET

Cumulative

FOR NSF USE ONLY		
PROPOSAL NO.	DURATION (months) Proposed	Granted
AWARD NO.		

ORGANIZATION
Pragmatic C Software Corp.

PRINCIPAL INVESTIGATOR / PROJECT DIRECTOR
Steven J Meyer

A. SENIOR PERSONNEL: PI/PD, Co-PI's, Faculty and Other Senior Associates (List each separately with title, A.7. show number in brackets)	NSF Funded Person-months CAL	ACAD	SUMR	Funds Requested By proposer	Funds granted by NSF (if different)
1. **Steven J Meyer - president**	2.40	0.00	0.00	$ 18,720	$
2. **Andrew I Vanvick - technical staff**	3.40	0.00	0.00	12,600	
3.					
4.					
5.					
6. ( ) OTHERS (LIST INDIVIDUALLY ON BUDGET JUSTIFICATION PAGE)	0.00	0.00	0.00	0	
7. (**2**) TOTAL SENIOR PERSONNEL (1 - 6)	5.80	0.00	0.00	31,320	
B. OTHER PERSONNEL (SHOW NUMBERS IN BRACKETS)					
1. (**0**) POST DOCTORAL ASSOCIATES	0.00	0.00	0.00	0	
2. (**0**) OTHER PROFESSIONALS (TECHNICIAN, PROGRAMMER, ETC.)	0.00	0.00	0.00	0	
3. (**3**) GRADUATE STUDENTS				8,420	
4. (**0**) UNDERGRADUATE STUDENTS				0	
5. (**0**) SECRETARIAL - CLERICAL (IF CHARGED DIRECTLY)				0	
6. (**0**) OTHER				0	
TOTAL SALARIES AND WAGES (A + B)				39,740	
C. FRINGE BENEFITS (IF CHARGED AS DIRECT COSTS)				0	
TOTAL SALARIES, WAGES AND FRINGE BENEFITS (A + B + C)				39,740	
D. EQUIPMENT (LIST ITEM AND DOLLAR AMOUNT FOR EACH ITEM EXCEEDING $5,000.)					
TOTAL EQUIPMENT				0	
E. TRAVEL 1. DOMESTIC (INCL. CANADA, MEXICO AND U.S. POSSESSIONS)				1,480	
2. FOREIGN				0	
F. PARTICIPANT SUPPORT COSTS					
1. STIPENDS $ 0					
2. TRAVEL 0					
3. SUBSISTENCE 0					
4. OTHER 0					
(**0**) TOTAL PARTICIPANT COSTS				0	
G. OTHER DIRECT COSTS					
1. MATERIALS AND SUPPLIES				1,080	
2. PUBLICATION COSTS/DOCUMENTATION/DISSEMINATION				0	
3. CONSULTANT SERVICES				0	
4. COMPUTER SERVICES				0	
5. SUBAWARDS				0	
6. OTHER				6,000	
TOTAL OTHER DIRECT COSTS				7,080	
H. TOTAL DIRECT COSTS (A THROUGH G)				48,300	
I. INDIRECT COSTS (F&A)(SPECIFY RATE AND BASE)					
TOTAL INDIRECT COSTS (F&A)				0	
J. TOTAL DIRECT AND INDIRECT COSTS (H + I)				48,300	
K. FEE (IF REQUESTED MAXIMUM = 7% OF J)				3,381	
L. TOTAL COST AND FEE (J + K)				$ 51,681	$

PI/PD NAME
Steven J Meyer

ORG. REP. NAME*
Steven meyer

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INDIRECT COST RATE VERIFICATION		
Date Checked	Date Of Rate Sheet	Initials - ORG

C***ELECTRONIC SIGNATURES REQUIRED ONLY FOR REVISED BUDGET**